NuMicro® Family

1T 8051-based Microcontroller

MS51 Series

MS51EB0AE

MS51FC0AE

MS51XC0BE

MS51EC0AE

MS51TC0AE

MS51PC0AE

Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The MS51 is an embedded Flash type, 8-bit high performance 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced.

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE contains a 32 Kbytes and MS51EB0AE contains a 16 Kbytes of main Flash called APROM, in which the contents of User Code resides. The MS51 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. IAP also makes it possible to configure any block of User Code array to be used as non-volatile data storage, which is written by IAP and read by IAP or MOVC instruction. There is an additional Flash called LDROM, in which the Boot Code normally resides for carrying out In-System-Programming (ISP). The LDROM size is configurable with a maximum of 4 Kbytes. To facilitate programming and verification, the Flash allows to be programmed and read electronically by parallel Writer or In-Circuit-Programming (ICP). Once the code is confirmed, user can lock the code for security.

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE provides rich peripherals including 256 bytes of SRAM, 2 Kbytes of auxiliary RAM (XRAM), Up to 29 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, three ISO 7816-3 interfaces, one SPI, one I^2C, six basic PWM output channels, six enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and one 12-bit ADC. The peripherals are equipped with 24 sources with 4-level-priority interrupts capability.

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE series is equipped with three clock sources and supports switching on-the-fly via software. The three clock sources include external clock input, 10 kHz internal oscillator, and one 16 MHz internal precise oscillator that is factory trimmed to ±1% at room temperature. The MS51 provides additional power monitoring detection such as power-on reset and 4-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE microcontroller operation consumes a very low power with two economic power modes to reduce power consumption — Idle and Power-down mode, which are software selectable. Idle mode turns off the CPU clock but allows continuing peripheral operation. Power-down mode stops the whole system clock for minimum power consumption. The system clock of the MS51 can also be slowed down by software clock divider, which allows for a flexibility between execution performance and power consumption.

With high performance CPU core and rich well-designed peripherals, the MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE benefits to meet a general purpose, home appliances, or motor control system accomplishment.

2 FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller. • Instruction set fully compatible with MCS-51. • 4-priority-level interrupts capability. • Dual Data Pointers (DPTRs).
Power on Reset (POR)	• POR with 1.15V threshold voltage level
Brown-out Detector (BOD)	• 4-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 2.7V / 2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM
Memories	
Flash	• Up to 32 KBytes of APROM for User Code. • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 Bytes on-chip RAM. • Additional 2 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation
Internal Clock Source	• Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 ˚C, 3.3 V), ±2% in -20~105˚C. • Selectable 24 MHz high-speed internal oscillator (HIRC).

	• 10 kHz low-speed internal oscillator (LIRC) calibrating to ±1% by software from high-speed internal oscillator
Timers	
16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. • One 16-bit Timer2 with three-channel input capture module and 9 input pin can be selected. • One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
Watchdog	• 6-bit free running up counter for WDT time-out interval. • Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC). • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval. • Clock sources from LIRC • Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value. • Supports Interrupt
PWM	• Up To 12 output pins can be selected • Supports maximum clock source frequency up to 24 MHz • Supports up to Three PWM modules, each module provides 6 output channels. • Supports independent mode for PWM output • Supports complementary mode for 3 complementary paired PWM output channels • Dead-time insertion with 8-bit resolution • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • Supports brake function • Supports trigger ADC on the following events
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD}. • 12-bit resolution and 10-bit accuracy is guaranteed. • Up to 8 single-end analog input channels • 1 internal channels, they are band-gap voltage (VBG). • Maximum ADC peripheral clock frequency is 1 MHz.

	• Up to 500 KSPS sampling rate. • Software Write 1 to ADCS bit. • External pin (STADC) trigger • PWM trigger. • Support continues convert function auto store the A/D conversion result in XRAM.
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0, UART1, • Up to three sets ISO 7816-3 device configuration as UART • UART baud rate clock from HIRC or HXT. • Full-duplex asynchronous communications • Programmable 9th bit. • TXD and RXD pins of UART0 exchangeable via software.
I²C	• 1 sets of I²C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps). • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Supports hold time programmable
SPI	• 1 sets of SPI devices • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • slave mode up to 12 MHz
ISO-7816	• Up to three sets ISO 7816-3 device • Supports ISO 7816-3 compliant T=0, T=1 • Supports full-duplex UART mode.
GPIO	• Four I/O modes: • Quasi-bidirectional mode • Push-Pull Output mode • Open-Drain Output mode • Input only with high impendence mode • Schmitt trigger input / TTL mode selectable. • Each I/O pin configured as interrupt source with edge/level trigger setting

	• Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$. • Supports high drive and high sink current I/O • I/O pin internal pull-up or pull-down resistor enabled in input mode. • Maximum I/O Speed is 24 MHz • Enabling the pin interrupt function will also enable the wake-up function
ESD & EFT	
ESD	• HBM pass 8 kV
EFT	• > ± 4.4 kV
Latch-up	• 150 mA pass

3 PARTS INFORMATION

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1 MS51 Series Package Type

	MSOP10	TSSOP14	TSSOP20	QFN20	TSSOP28	LQFP32	QFN33
Part No.	MS51BA9AE	MS51DA9AE	MS51FB9AE MS51FC0AE	MS51XB9AE MS51XB9BE MS51XC0BE	MS51EC0AE MS51EB0AE	MS51PC0AE	MS51TC0AE

3.2 MS51 Series Selection Gude

Part Number	Flash (KB)	SRAM (KB)	LDROM (KB) [1]	I/O	Timer	PWM	Connectivity				ADC(12-Bit)	Package
							ISO 7816-3 [2]	UART	SPI	I2C		
MS51BA9AE	8	1	4	8	4	5	-	2	-	1	5-ch	MSOP10
MS51DA9AE	8	1	4	12	4	5	-	2	1	1	8-ch	TSSOP14
MS51XB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20[3]
MS51XB9BE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20[3]
MS51FB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20
MS51EB0AE	16	2	4	26	4	11	3	2	1	1	15-ch	TSSOP28
MS51FC0AE	32	2	4	18	4	11	2	2	1	1	10-ch	TSSOP20
MS51XC0BE	32	2	4	18	4	8	2	2	1	1	10-ch	QFN20
MS51EC0AE	32	2	4	26	4	11	3	2	1	1	15-ch	TSSOP28
MS51PC0AE	32	2	4	30	4	12	3	2	1	1	15-ch	LQFP32
MS51TC0AE	32	2	4	30	4	12	3	2	1	1	15-ch	QFN33

Note:

1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.
2. ISO 7816-3 configurable as UART function, GPIO defined as UART2 ~ UART4.
3. Detailed package information please refer to MS51FB9AE / MS51XB9AE / MS51XB9BE series document.
4. This document is only for MS51EB0AE/MS51FC0AE/MS51XC0BE/MS51EC0AE/MS51TC0AE/MS51PC0AE products.

3.3 MS51 Series Selection Code

MS	51	F	B	9	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
1T 8051 Industry	51: Base	B: MSOP10 (3x3 mm) D: TSSOP14 (4.4x5.0 mm) E: TSSOP28 (4.4x9.7 mm) F: TSSOP20 (4.4x6.5 mm) I: SOP8 (4x5 mm) O: SOP20 (300 mil) P: LQFP32 (7x7 mm) T: QFN33 (4x4 mm) U: SOP28 (300 mil) X: QFN20 (3x3mm)	A: 8 KB B: 16 KB C: 32 KB	0: 2 KB 1: 4 KB 2: 8/12 KB 3: 16 KB 6: 32 KB 8: 64 KB 9: 1 KB A: 96 KB		E:-40 ~ 105° C

4 PIN CONFIGURATION

Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 MS51EB0AE/MS51FC0AE/MS51XC0BE/MS51EC0AE/MS51TC0AE/MS51PC0AE Multi Function Pin Diagram

4.1.1 QFN 33-pin Package Pin Diagram

Corresponding Part Number: MS51TC0AE

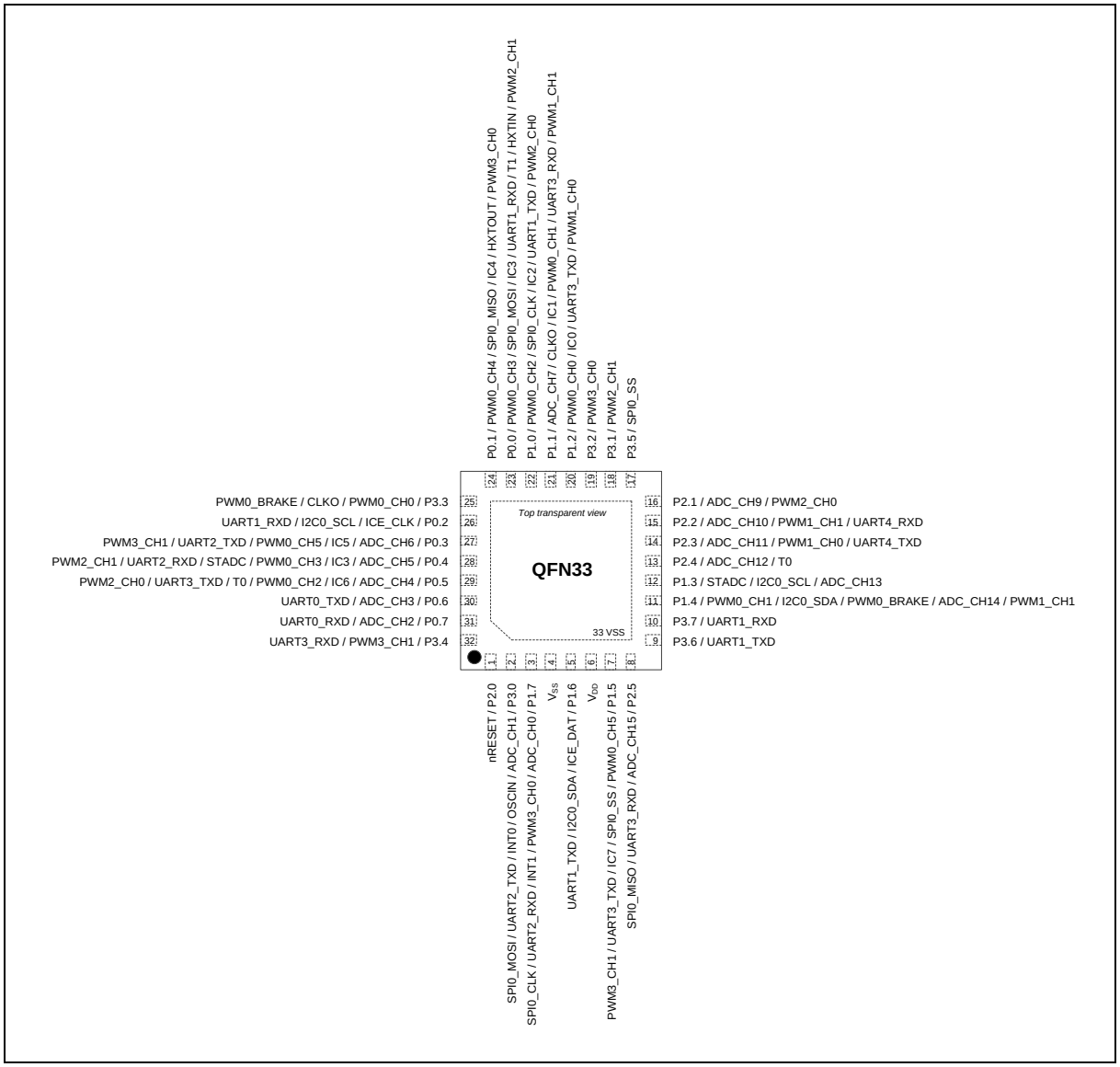


Figure 4.1-1 Pin Assignment of LQFP-32 Package

4.1.2 LQFP 32-pin Package Pin Diagram

Corresponding Part Number: MS51PC0AE

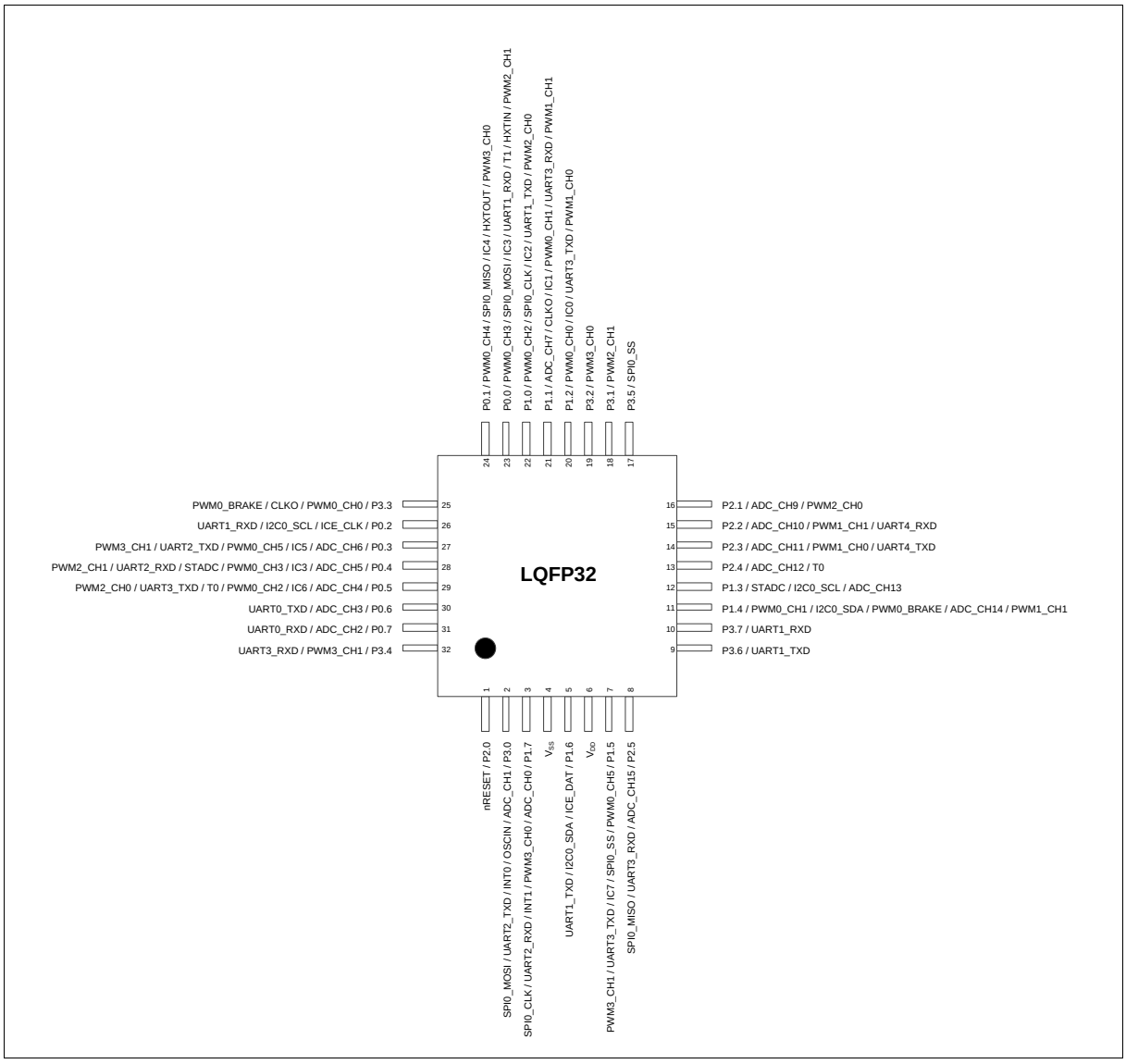


Figure 4.1-2 Pin Assignment of LQFP-32 Package

4.1.3 TSSOP 28-pin Package Pin Diagram

Corresponding Part Number: MS51EC0AE

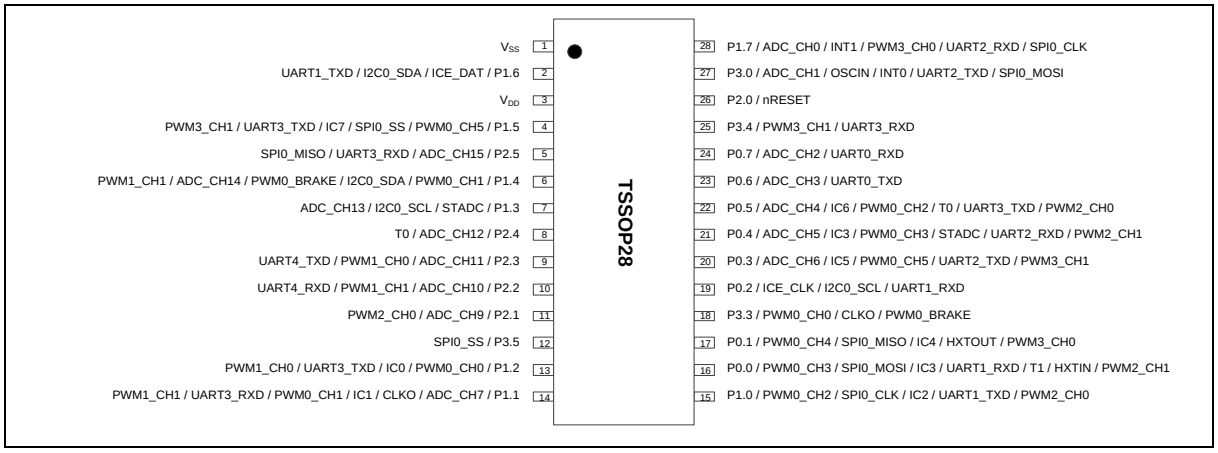


Figure 4.1-3 Pin Assignment of TSSOP28 Package

4.1.4 TSSOP 20-pin Package Pin Diagram

Corresponding Part Number: MS51FC0AE

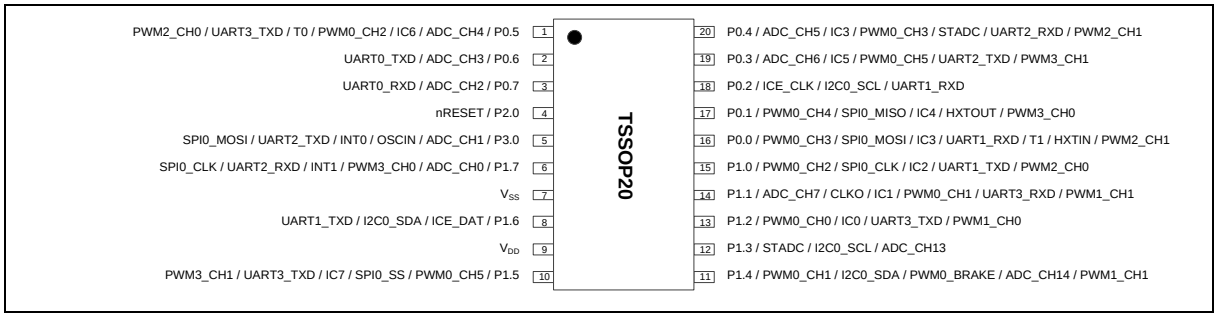


Figure 4.1-4 Pin Assignment of TSSOP20 Package

4.1.5 QFN 20-pin Package Pin Diagram

Corresponding Part Number: MS51XC0BE

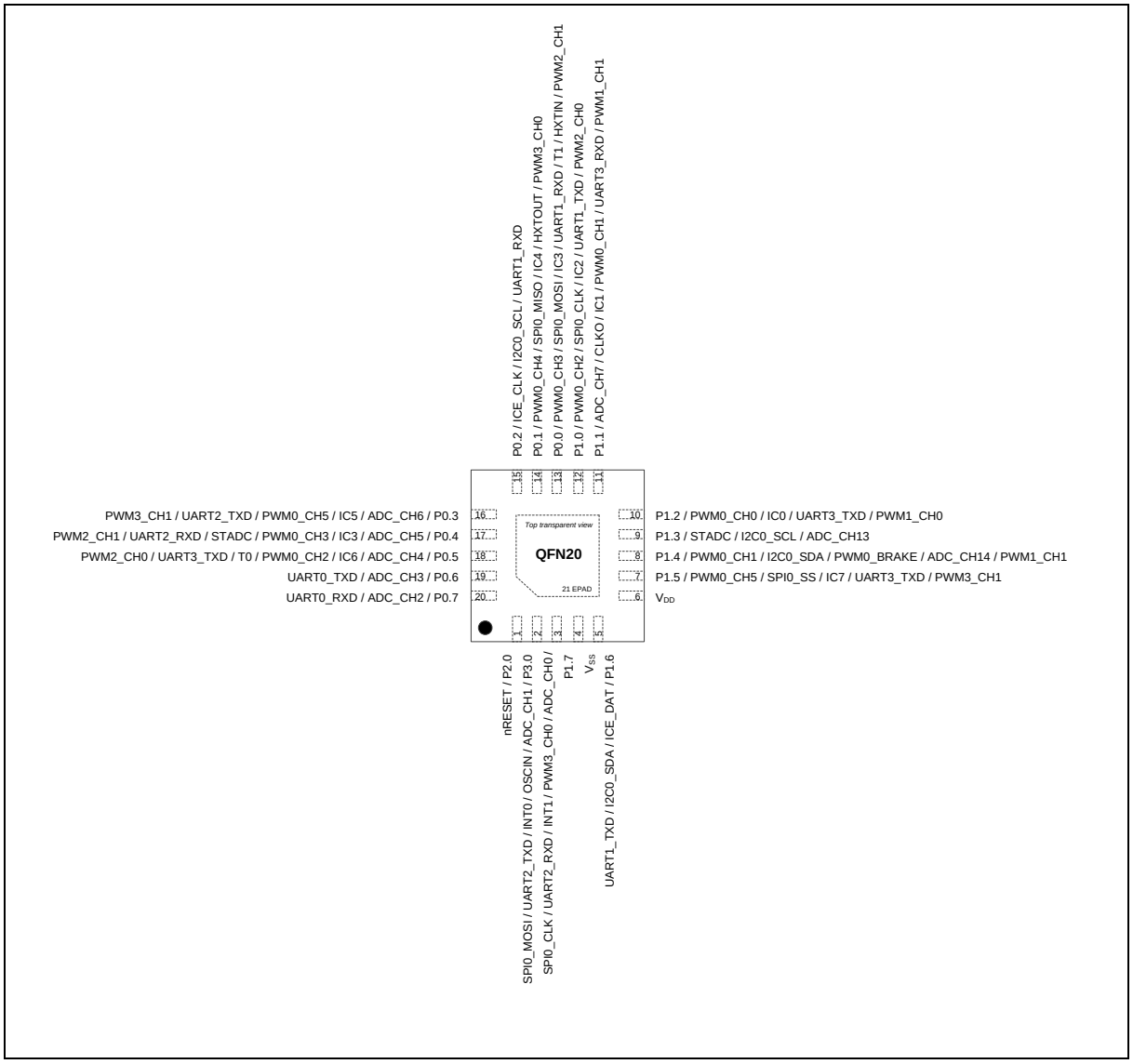


Figure 4.1-5 Pin Assignment of QFN20 Package

4.2 MS51EB0AE/MS51FC0AE/MS51XC0BE/MS51EC0AE/MS51TC0AE/MS51PC0AE Pin Description

Pin Number				Symbol	Multi-Function Description[1]
MS51XC0BE QFN 20	MS51FC0AE TSSOP20	MS51EC0AE TSSOP28	MS51PC0AE LQFP 32 MS51TC0AE QFN 33		
6	9	3	6	**VDD**	Supply voltage V_{DD} for operation.
4	7	1	4	**VSS**	Ground potential.
13	16	16	23	**P0.0**	Port 0 bit 0.
				PWM0_CH3	PWM0 output channel 3.
				PWM2_CH1	PWM2 output channel 1.
				IC3	Input capture channel 3.
				SPI0_MOSI	SPI master output/slave input.
				UART1_RXD	UART1 receive input.
				XT1_IN	External 4~24 MHz (high speed) crystal input pin.
				OSCIN	If the EXTEN[1:0] = 10b, OSCIN is the external clock input pin.
				T1	External count input to Timer/Counter 1 or its toggle output.
14	17	17	24	**P0.1**	Port 0 bit 1.
				PWM0_CH4	PWM0 output channel 4.
				PWM3_CH0	PWM3 output channel 0.
				IC4	Input capture channel 4.
				SPI0_MISO	SPI master input/slave output.
				XT1_OUT	External 4~24 MHz (high speed) crystal output pin.
15	18	19	26	**P0.2**	Port 0 bit 2.
				I2C0_SCL	I^2C clock.
				UART1_RXD	UART1 receive input.
				ICE_CLK	ICE / ICP clock input. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
16	19	20	27	**P0.3**	Port 0 bit 3.
				ADC_CH6	ADC input channel 6.
				PWM0_CH5	PWM0 output channel5
				PWM3_CH1	PWM3 output channel1
				IC5	Input capture channel 5.
				UART2_TXD	UART2 transmit data output.
				SC0_CLK	Smart Card 0 clock pin
17	20	21	28	**P0.4**	Port 0 bit 4.
				ADC_CH5	ADC input channel 5.
				PWM0_CH3	PWM0 output channel 3.
				PWM2_CH1	PWM2 output channel 1.
				IC3	Input capture channel 3.
				UART2_RXD	UART2 receive input.
				SC0_DAT	Smart Card 0 data pin
				STADC	External start ADC trigger
18	1	22	29	**P0.5**	Port 0 bit 5.
				ADC_CH4	ADC input channel 4.
				PWM0_CH2	PWM0 output channel 2.
				PWM2_CH0	PWM2 output channel 0.
				IC6	Input capture channel 6.
				UART3_TXD	UART3 transmit data output.
				SC1_CLK	Smart card clock pin.

Pin Number				Symbol	Multi-Function Description[1]
MS51XC0BE QFN 20	MS51FC0AE TSSOP20	MS51EC0AE TSSOP28	MS51PC0AE LQFP 32 MS51TC0AE QFN 33		
				T0	External count input to Timer/Counter 0 or its toggle output.
19	2	23	30	**P0.6**	Port 0 bit 6.
				ADC_CH3	ADC input channel 3.
				UART0_TXD	UART0 transmit data output.
20	3	24	31	**P0.7**	Port 0 bit 7.
				ADC_CH2	ADC input channel 2.
				UART0_RXD	UART0 transmit data output.
12	15	15	22	**P1.0**	Port 1 bit 0.
				PWM0_CH2	PWM0 output channel 2.
				PWM2_CH0	PWM2 output channel 0.
				IC2	Input capture channel 2.
				SPI0_CLK	SPI0 clock.
				UART1_TXD	UART1 receive input.
11	14	14	21	**P1.1**	Port 1 bit 1
				ADC_CH7	ADC input channel 7.
				PWM0_CH1	PWM0 output channel 1.
				PWM1_CH1	PWM1 output channel 1.
				IC1	Input capture channel 1.
				UART3_RXD	UART3 receive input.
				SC1_DAT	Smart Card 1 data pin.
				CLKO	System clock output.
10	13	13	20	**P1.2**	Port 1 bit 2.
				PWM0_CH0	PWM0 output channel 0.
				PWM1_CH0	PWM1 output channel 0.
				IC0	Input capture channel 0.
				UART3_TXD	UART3 transmit data output.
				SC1_CLK	Smart Card 1 clock pin.
9	12	7	12	**P1.3**	Port 1 bit 3.
				ADC_CH13	ADC input channel 13.
				I2C0_SCL	I^2C0 clock.
				STADC	External start ADC trigger
8	11	6	11	**P1.4**	Port 1 bit 4.
				ADC_CH14	ADC input channel 14.
				PWM0_CH1	PWM0 output channel 1.
				PWM1_CH1	PWM1 output channel 1.
				I2C0_SDA	I^2C0 data.
				PWM0_BRAKE	PWM0 Fault Brake input.
7	10	4	7	**P1.5**	Port 1 bit 5.
				PWM0_CH5	PWM0 output channel 5.
				PWM3_CH1	PWM3 output channel 1.
				IC7	Input capture channel 7.
				SPI0_SS	SPI0 slave select input.
				UART3_TXD	UART3 transmit data output.
				SC1_CLK	Smart card 2 clock pin
5	8	2	5	**P1.6**	Port 1 bit 6.
				I2C0_SDA	I^2C0 data.
				UART1_TXD	UART1 transmit data output.
				ICE_DAT	ICE data input or output. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
3	6	28	3	**P1.7**	Port 1 bit 7.

Pin Number				Symbol	Multi-Function Description[1]
MS51XC0BE QFN 20	MS51FC0AE TSSOP20	MS51EC0AE TSSOP28	MS51PC0AE LQFP 32 MS51TC0AE QFN 33		
				ADC_CH0	ADC input channel 0.
				PWM3_CH0	PWM3 output channel 0.
				SPI0_CLK	SPI0 clock.
				UART2_RXD	UART2 receive input.
				SC0_DAT	Smart Card 0 data pin
				INT1	External interrupt 1 input.
1	4	26	1	**P2.0**	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
				nRESET	It is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to VSS. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
-	-	11	16	**P2.1**	Port 2 bit 1.
				ADC_CH9	ADC input channel 9.
				PWM2_CH0	PWM2 output channel 0.
-	-	10	15	**P2.2**	Port 2 bit 2.
				ADC_CH10	ADC input channel 10.
				PWM1_CH1	PWM1 output channel 1.
				UART4_RXD	UART4 receive input.
				SC2_DAT6	Smart card 2 data pin
-	-	9	14	**P2.3**	Port 2 bit 3.
				ADC_CH11	ADC input channel 11.
				PWM1_CH0	PWM1 output channel 0.
				UART4_TXD	UART4 transmit data output.
				SC2_CLK6	Smart card 2 clock pin
-	-	8	13	**P2.4**	Port 2 bit 4.
				ADC_CH12	ADC input channel 12.
				T0	External count input to Timer/Counter 0 or its toggle output.
-	-	5	8	**P2.5**	Port 2 bit 5.
				ADC_CH15	ADC input channel 15.
				SPI0_MISO	SPI master input/slave output.
				UART3_RXD	UART3 receive input.
				SC1_DAT6	Smart card 1 data pin
2	5	27	2	**P3.0**	Port 3 bit 0.
				ADC_CH1	ADC input channel 1.
				PWM2_CH1	PWM2 output channel 1.
				PI0_MOSI	SPI master output/slave input.
				UART2_TXD	UART2 transmit data output.
				SC0_CLK6	Smart card 0 clock pin
				INT0	External interrupt 0 input.
				OSCIN	If the EXTEN[1:0] = 11b, OSCIN is the external clock input pin.
-	-	-	18	**P3.1**	Port 3 bit 1.
				PWM2_CH1	PWM2 output channel 1.
-	-	-	19	**P3.2**	Port 3 bit 2.
				PWM3_CH0	PWM3 output channel 0.
-	-	18	25	**P3.3**	Port 3 bit 3.
				PWM0_CH0	PWM3 output channel 0.
				CLK_OUT	System clock output.

Pin Number				Symbol	Multi-Function Description[1]
MS51XC0BE QFN 20	MS51FC0AE TSSOP20	MS51EC0AE TSSOP28	MS51PC0AE LQFP 32 MS51TC0AE QFN 33		
				PWM0_BRAKE	PWM0 Fault Brake input.
-	-	25	32	**P3.4**	Port 3 bit 4.
				PWM3_CH1	PWM3 output channel 0.
				UART3_RXD	UART3 receive input.
				SC1_DAT	Smart card 0 data pin
-	-	12	17	**P3.5**	Port 3 bit 5.
				SPI0_SS	SPI0 slave select input.
-	-	-	9	**P3.6**	Port 3 bit 6.
				UART1_TXD	UART1 transmit data output.
-		-	10	**P3.7**	Port 3 bit 7.
				UART1_RXD	UART1 receive input.
21	-	-	-	**EPAD**	Exposed PAD (floating)

Note:

1. All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
2. UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).
3. [I2C] alternate function remapping option. I2C pins is software switched by I2CPX (I2CON.0).
4. [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
5. PIOx register decides which pins are PWM or GPIO.
6. UART2_TXD and UART2_RXD pin is defined by AUXR2 register. UART3_TXD, UART3_RXD, UART4_TXD and UART4_RXD pin defined by AUXR3 register.

5 BLOCK DIAGRAM

5.1 MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE Block Diagram

Figure 5.1-1 Functional Block Diagram shows the MS51 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

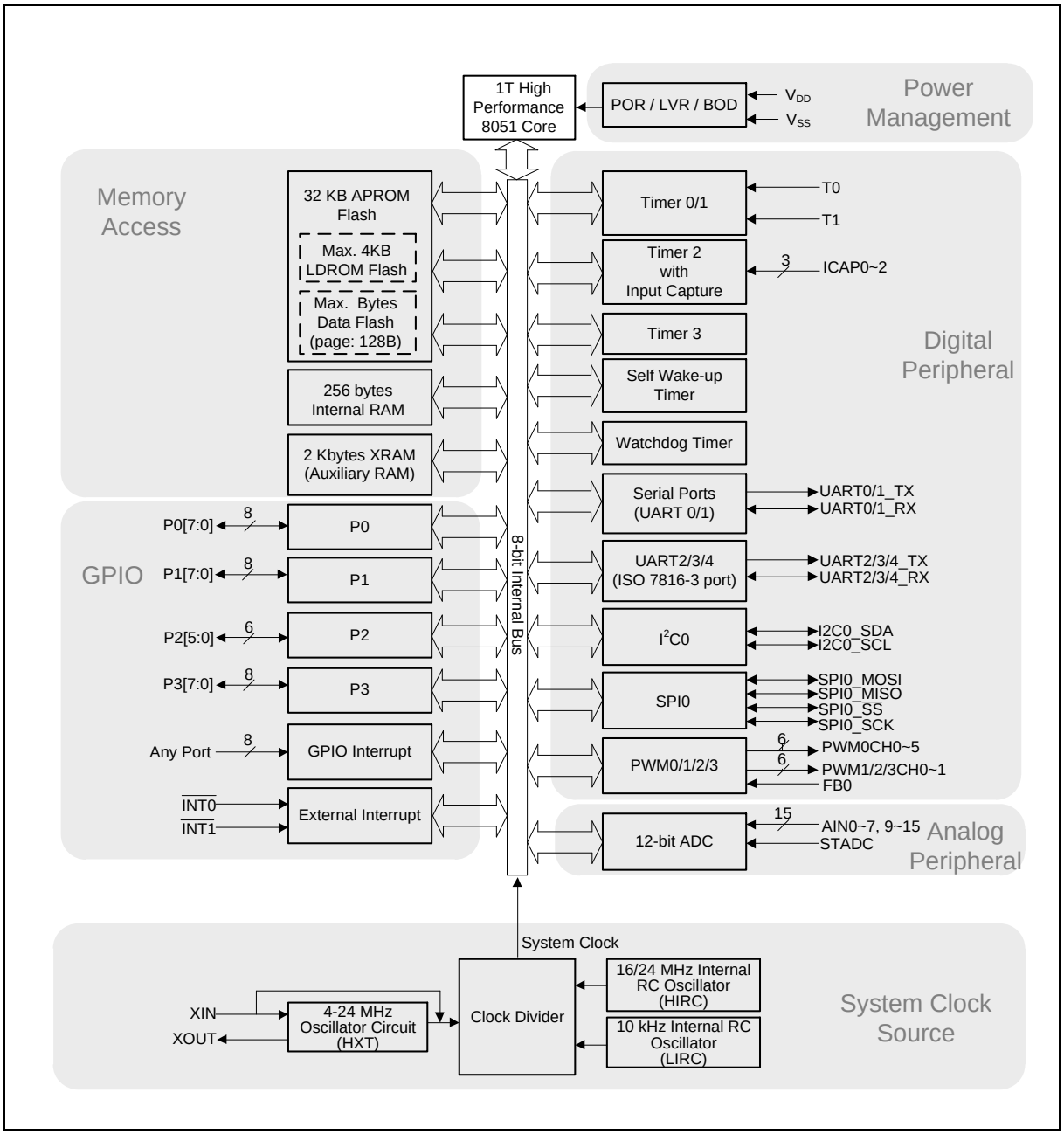


Figure 5.1-1 Functional Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Memory Organization

6.1.1 Overview

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In MS51, there are 256 bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the MS51 provides another on-chip 2 Kbytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded Flash, functioning as Program Memory, is divided into three blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 bytes. The Flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

6.2 Flash Memory Control

6.2.1 Reset

6.2.1.1 Overview

The MS51 has several options to place device in reset condition. It also offers the software flags to indicate the source, which causes a reset. In general, most SFR go to their Reset value irrespective of the reset condition, but there are several reset source indicating flags whose state depends on the source of reset. User can read back these flags to determine the cause of reset using software. There are five ways of putting the device into reset state. They are power-on reset, brown-out reset, external reset, WDT reset, and software reset.

6.2.1.2 Power-On Reset (POR) and Low Voltage Reset (LVR)

The MS51 incorporates an internal power-on reset (POR) and a low voltage reset (LVR). During a power-on process of rising power supply voltage V_{DD}, the POR or LVR will hold the MCU in reset mode when V_{DD} is lower than the voltage reference thresholds. This design makes CPU not access program Flash while the V_{DD} is not adequate performing the Flash reading. If an undetermined operating code is read from the program Flash and executed, this will put CPU and even the whole system in to an erroneous state. After a while, V_{DD} rises above the threshold where the system can work, the selected oscillator will start and then program code will execute from 0000H. At the same time, a power-on flag POF (PCON.4) will be set 1 to indicate a cold reset, a power-on process complete. Note that the contents of internal RAM will be undetermined after a power-on. It is recommended that user gives initial values for the RAM block.

The POF is recommended to be cleared to 0 via software to check if a cold reset or warm reset performed after the next reset occurs. If a cold reset caused by power off and on, POF will be set 1 again. If the reset is a warm reset caused by other reset sources, POF will remain 0. User may take a different course to check other reset flags and deal with the warm reset event. For detailed electrical characteristics, refer to the table 35-7 and 35-8.

PCON – Power Control

Register	SFR Address	Reset Value
PCON	87H, All pages	POR: 0001_0000b Others: 000U _0000b

7	6	5	4	3	2	1	0
SMOD	SMOD0	LPR	POF	GF1	GF0	PD	IDL
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
4	POF	Power-on reset flag This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

6.2.1.3 Brown-Out Reset

The brown-out detection circuit is used for monitoring the V_{DD} level during execution. When V_{DD} drops to the selected brown-out trigger level (V_{BOD}), the brown-out detection logic will reset the MCU if BORST

(BODCON0.2) setting 1. After a brown-out reset, BORF (BODCON0.1) will be set as 1 via hardware. BORF will not be altered by any reset other than a power-on reset or brown-out reset itself. This bit can be set or cleared by software.

BODCON0 – Brown-out Detection Control 0

Register	SFR Address	Reset Value
BODCON0	A3H, Page 0, TA protected	POR,CCCC XC0X b BOD, UUUU XU1X b Others,UUUU XUUX b

7	6	5	4	3	2	1	0
BODEN	BOV[2:0]			BOF	BORST	BORF	BOS
R/W	R/W			R/W	R/W	R/W	R

Bit	Name	Description
1	BORF	Brown-out reset flag When the MCU is reset by brown-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.

6.2.1.4 External Reset and Hard Fault Reset

The external reset pin $\overline{\text{RST}}$ is an input with a Schmitt trigger. An external reset is accomplished by holding the $\overline{\text{RST}}$ pin low for at least 24 system clock cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus, the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain as long as $\overline{\text{RST}}$ pin is low. After the $\overline{\text{RST}}$ high is removed, the MCU will exit the reset state and begin code executing from address 0000H. If an external reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops system clock, the reset signal will asynchronously cause the system clock resuming. After the system clock is stable, MCU will enter the reset state.

There is a RSTPINF (AUXR0.6) flag, which indicates an external reset took place. After the external reset, this bit will be set as 1 via hardware. RSTPINF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software.

Hard Fault reset will occur if CPU fetches instruction address over Flash size, HardF (AUXR0.5) flag will be set via hardware. HardF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software. If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled. Only HardF flag be asserted.

AUXR1 – Auxiliary Register 1

Register	SFR Address	Reset Value
AUXR1	A2H , Page 0	POR: 0000 0000b, Software reset: 1U00 0000b, nRESET pin: U100 0000b, Others: UUU0 0000b

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	SLOW	GF2	UART0PX	0	DPS
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit	Name	Description
6	RSTPINF	External reset flag When the MCU is reset by the external reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.
5	HardF	Hard Fault reset flag Once CPU fetches instruction address over Flash size while EHFI (EIE1.4)=0, MCU will reset and this bit will be set via hardware. It is recommended that the flag be cleared via software. **Note:** If MCU run in OCD debug mode and OCDEN = 0, Hard fault reset will disable. Only HardF flag be asserted.

6.2.1.5 Watchdog Timer Reset

The WDT is a free running timer with programmable time-out intervals and a dedicated internal clock source. User can clear the WDT at any time, causing it to restart the counter. When the selected time-out occurs but no software response taking place for a while, the WDT will reset the system directly and CPU will begin execution from 0000H.

Once a reset due to WDT occurs, the WDT reset flag WDTRF (WDCON.3) will be set. This bit keeps unchanged after any reset other than a power-on reset or WDT reset itself. User can clear WDTRF via software.

WDCON – Watchdog Timer Control

Register	SFR Address	Reset Value
WDCON	AAH, Page 0, TA protected	POR 0000_0111 b WDT 0000_1UUU b Others 0000_UUUU b

7	6	5	4	3	2	1	0
WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Bit	Name	Description
3	WDTRF	WDT reset flag When the CPU is reset by WDT time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software after reset.

6.2.1.6 Software Reset

The MS51 provides a software reset, which allows the software to reset the whole system just similar to an external reset, initializing the MCU as it reset state. The software reset is quite useful in the end of an ISP progress. For example, if an ISP of Boot Code updating User Code finishes, a software reset can be asserted to re-boot CPU to execute new User Code immediately. Writing 1 to SWRST (CHPCON.7) will trigger a software reset. Note that this bit is writing TA protection. The instruction that sets the SWRST bit is the last instruction that will be executed before the device reset. See demo code below.

If a software reset occurs, SWRF (AUXR0.7) will be automatically set by hardware. User can check it as the reset source indicator. SWRF keeps unchanged after any reset other than a power-on reset or software reset itself. SWRF can be cleared via software.

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	OCDPWM	OCDEN	-	RPD	LOCK	-
R/W	-	R/W	R/W	-	R/W	R/W	-

Factory default value: 1111 1111b

Bit	Name	Description
7	CBS	CONFIG boot select This bit defines from which block that MCU re-boots after resets except software reset. 1 = MCU will re-boot from APROM after resets except software reset. 0 = MCU will re-boot from LDROM after resets except software reset.
5	OCDPWM	PWM output state under OCD halt This bit decides the output state of PWM when OCD halts CPU. 1 = Tri-state pins those are used as PWM outputs. 0 = PWM continues. Note that this bit is valid only when the corresponding PIO bit of PWM channel is set as 1.
4	OCDEN	OCD enable 1 = OCD Disabled. 0 = OCD Enabled. **Note:** If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled and only Hard F flag be asserted.
2	RPD	Reset pin disable 1 = The reset function of P2.0/Nrst pin Enabled. P2.0/Nrst functions as the external reset pin. 0 = The reset function of P2.0/Nrst pin Disabled. P2.0/Nrst functions as an input-only pin P2.0.
1	LOCK	Chip lock enable 1 = Chip is unlocked. Flash Memory is not locked. Their contents can be read out through a parallel Writer/ICP programmer. 0 = Chip is locked. Whole Flash Memory is locked. Their contents read through a parallel Writer or ICP programmer will be all blank (FFH). Programming to Flash Memory is invalid. Note that CONFIG bytes are always unlocked and can be read. Hence, once the chip is locked, the CONFIG bytes cannot be erased or programmed individually. The only way to disable chip lock is execute “whole chip erase”. However, all data within the Flash Memory and CONFIG bits will be erased when this procedure is executed. If the chip is locked, it does not alter the IAP function.

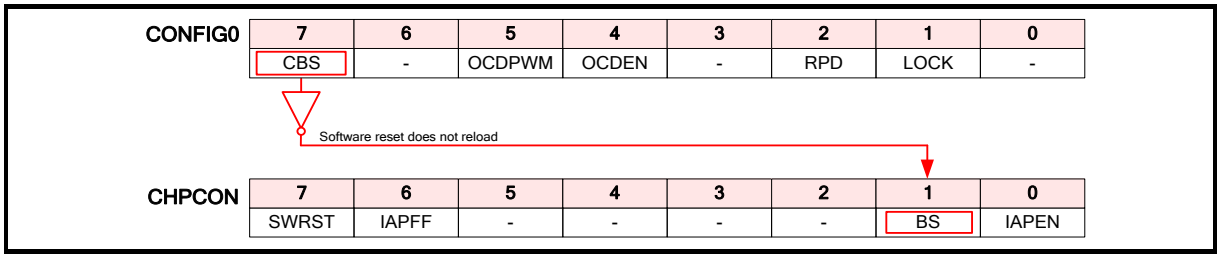


Figure 6.2-1 CONFIG0 Any Reset Reloading

CONFIG1

7	6	5	4	3	2	1	0
-	-	-	-	-	LDSIZE[2:0]		
-	-	-	-	-	R/W		

Factory default value: 1111 1111b

Bit	Name	Description
2:0	LDSIZE[2:0]	LDROM size select This field selects the size of LDROM. 111 = No LDROM. APROM is 32 Kbytes. 110 = LDROM is 1 Kbytes. APROM is 31 Kbytes. 101 = LDROM is 2 Kbytes. APROM is 30 Kbytes. 100 = LDROM is 3 Kbytes. APROM is 29 Kbytes. 0xx = LDROM is 4 Kbytes. APROM is 28 Kbytes.

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV[2:0]			BOIAP	CBORST	-	-
R/W	R/W			R/W	R/W	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7	CBODEN	CONFIG brown-out detect enable 1 = Brown-out detection circuit on. 0 = Brown-out detection circuit off.
5:4	CBOV[1:0]	CONFIG brown-out voltage select 11 = V_{BOD} is 2.2V. 10 = V_{BOD} is 2.7V. 01 = V_{BOD} is 3.7V. 00 = V_{BOD} is 4.4V.
3	BOIAP	Brown-out inhibiting IAP This bit decides whether IAP erasing or programming is inhibited by brown-out status. This bit is valid only when brown-out detection is enabled. 1 = IAP erasing or programming is inhibited if V_{DD} is lower than V_{BOD}. 0 = IAP erasing or programming is allowed under any workable V_{DD}.
2	CBORST	CONFIG brown-out reset enable This bit decides whether a brown-out reset is caused by a power drop below V_{BOD}. 1 = Brown-out reset Enabled. 0 = Brown-out reset Disabled.

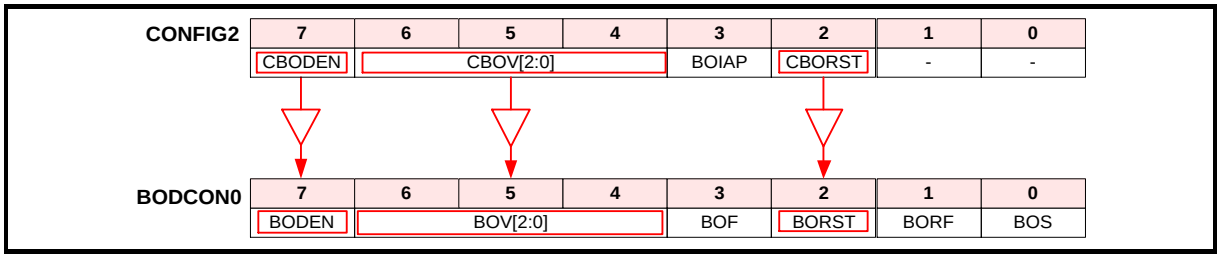


Figure 6.2-2 CONFIG2 Power-On Reset Reloading

CONFIG4

7	6	5	4	3	2	1	0
WDTEN[3:0]				-	-	-	-
R/W				-	-	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7:4	WDTEN[3:0]	WDT enable This field configures the WDT behavior after MCU execution. 1111 = WDT is Disabled. WDT can be used as a general purpose timer via software control. 0101 = WDT is Enabled as a time-out reset timer and it stops running during Idle or Power-down mode. Others = WDT is Enabled as a time-out reset timer and it keeps running during Idle or Power-down mode.
3:0	-	Reserved

6.3 General Purpose I/O (GPIO)

The MS51 has a maximum of 30 general purpose I/O pins which 29 bit-addressable general I/O pins grouped as 4 ports, P0 to P3, and 1 input only pin as P20. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, whereas a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

6.4 Timer

6.4.1 Timer/Counter 0 And 1

6.4.1.1 Overview

Timer/Counter 0 and 1 on MS51 are two 16-bit Timers/Counters. Each of them has two 8-bit registers those form the 16-bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similarly Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts the system clock cycles. The timer clock is 1/12 of the system clock (F_{SYS}) for standard 8051 capability or direct the system clock for enhancement, which is selected by T0M (CKCON.3) bit for Timer 0 and T1M (CKCON.4) bit for Timer 1. In the “Counter” mode, the countering register increases on the falling edge of the external input pin T0. If the sampled value is high in one clock cycle and low in the next, a valid 1-to-0 transition is recognized on T0 or T1 pin.

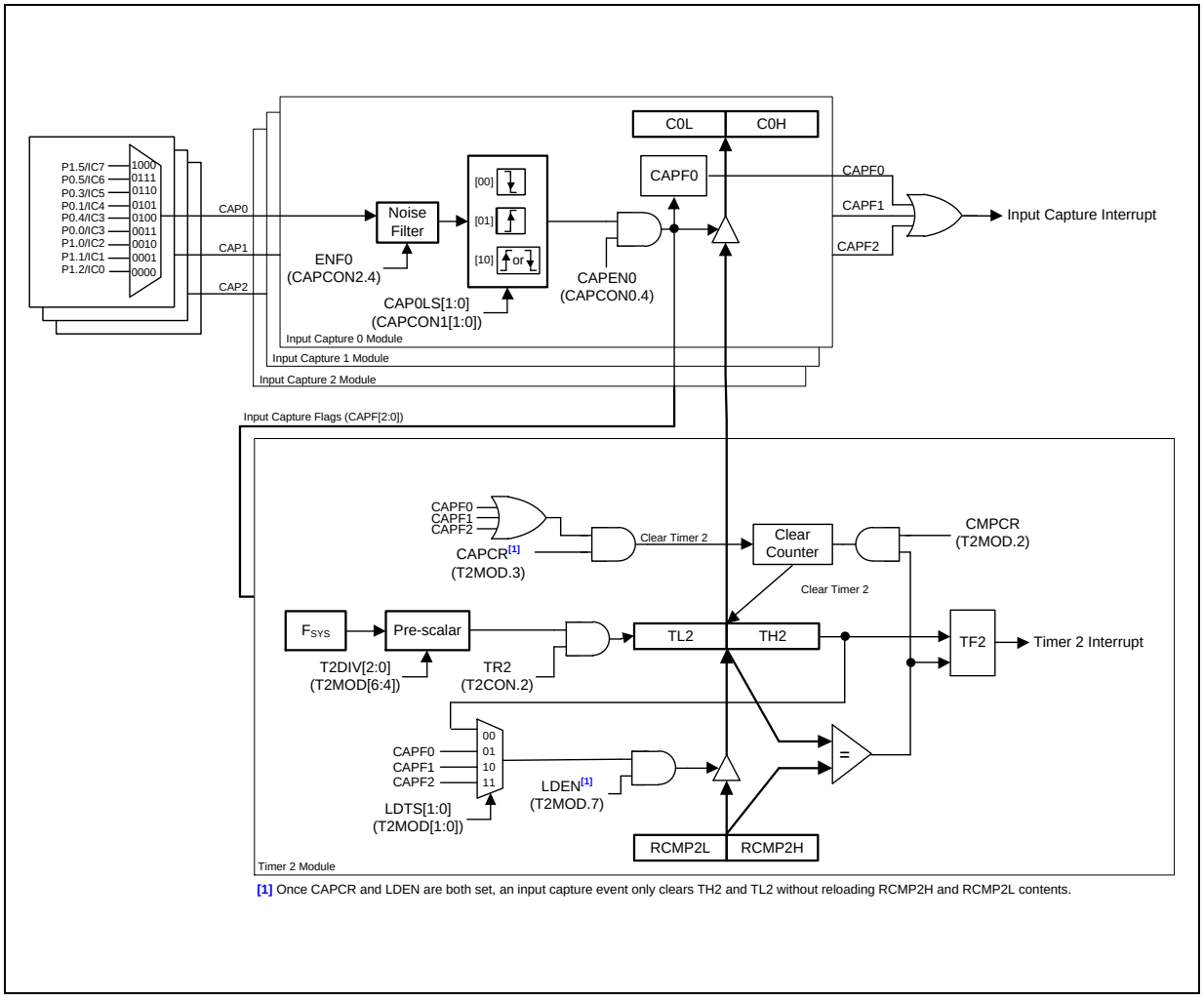
The Timers 0 and 1 can be configured to automatically to toggle output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the CKCON register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be logic 1 prior to the first timer overflow when this mode is turned on. In order for this mode to function, the C/$\overline{T}$ bit should be cleared selecting the system clock as the clock source for the timer.

Note that the TH0 (TH1) and TL0 (TL1) are accessed separately. It is strongly recommended that in mode 0 or 1, user should stop Timer temporally by clearing TR0 (TR1) bit before reading from or writing to TH0 (TH1) and TL0 (TL1). The free-running reading or writing may cause unpredictable result.

6.4.2 Timer2 And Input Capture

6.4.2.1 Overview

Timer 2 is a 16-bit up counter cascaded with TH2, the upper 8 bits register, and TL2, the lower 8 bit register. Equipped with RCMP2H and RCMP2L, Timer 2 can operate under compare mode and auto-reload mode selected by CM/$\overline{RL2}$ (T2CON.0). An 3-channel input capture module makes Timer 2 detect and measure the width or period of input pulses. The results of 3 input captures are stores in C0H and C0L, C1H and C1L, C2H and C2L individually. The clock source of Timer 2 is from the system clock pre-scaled by a clock divider with 8 different scales for wide field application. The clock is enabled when TR2 (T2CON.2) is 1, and disabled when TR2 is 0. The following registers are related to Timer 2 function.



[1] Once CAPCR and LDEN are both set, an input capture event only clears TH2 and TL2 without reloading RCMP2H and RCMP2L contents.

Figure 6.4-1 Timer 2 Block Diagram

6.4.3 Timer 3

6.4.3.1 Overview

Timer 3 is implemented simply as a 16-bit auto-reload, up-counting timer. The user can select the pre-scale with T3PS[2:0] (T3CON[2:0]) and fill the reload value into RH3 and RL3 registers to determine its overflow rate. User then can set TR3 (T3CON.3) to start counting. When the counter rolls over FFFFH, TF3 (T3CON.4) is set as 1 and a reload is generated and causes the contents of the RH3 and RL3 registers to be reloaded into the internal 16-bit counter. If ET3 (EIE1.1) is set as 1, Timer 3 interrupt service routine will be served. TF3 is auto-cleared by hardware after entering its interrupt service routine.

Timer 3 can also be the baud rate clock source of both UARTs..

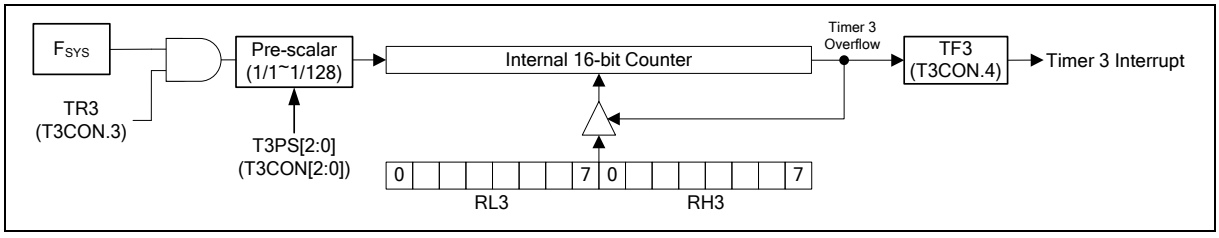


Figure 6.4-2 Timer 3 Block Diagram

6.5 Pulse Width Modulated (PWM)

6.5.1 Overview

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The MS51 PWM0 is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM0 output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

The MS51 PWM1/2/3 provide individual configurable period and duty. maximum 16-bit resolution output. Each of two PWM1/2/3 can be configured as one of independent mode, complementary mode, or synchronous mode.The PWM1/2/3 waveform can be edge-aligned or center-aligned with variable interrupt points.

PWM output pin define and enable control register table.

PWM Channel	Output Pin	Control register 1			Control register2		
		SFR Byte Name	Bit name	Value	SFR Byte Name	Bit name	Value
PWM0_CH0	P1.2	PIOCON0	PIO12	1	AUXR4[1:0]	PWM1C0P	00
	P3.3	PIOCON2	PIO33	1	-	-	-
PWM0_CH1	P1.1	PIOCON0	PIO11	1	AUXR4[3:2]	PWM1C1P	00
	P1.4	PIOCON1	PIO14	1	AUXR4[3:2]	PWM1C1P	00
PWM0_CH2	P0.5	PIOCON1	PIO05	1	AUXR4[5:4]	PWM2C0P	00
	P1.0	PIOCON0	PIO10	1	-	-	-
PWM0_CH3	P0.4	PIOCON1	PIO04	1	AUXR4[7:6]	PWM2C1P	00
	P0.0	PIOCON0	PIO00	1	AUXR4[7:6]	PWM2C1P	00
PWM0_CH4	P0.1	PIOCON0	PIO01	1	AUXR5[1:0]	PWM3C0P	00
PWM0_CH5	P0.3	PIOCON0	PIO03	1	AUXR5[3:2]	PWM3C1P	00
	P1.5	PIOCON1	PIO15	1	AUXR5[3:2]	PWM3C1P	00
PWM1_CH0	P2.3	PIOCON2	PIO23	1	AUXR4[1:0]	PWM1C0P	01
	P1.2	PIOCON0	PIO12	1			10
PWM1_CH1	P2.2	PIOCON2	PIO22	1	AUXR4[3:2]	PWM1C1P	01
	P1.4	PIOCON1	PIO14	1			10
	P1.1	PIOCON0	PIO11	1			11
PWM2_CH0	P2.1	PIOCON2	PIO21	1	AUXR4[5:4]	PWM2C0P	00
	P1.0	PIOCON0	PIO10	1			01
	P0.5	PIOCON1	PIO05	1			10
PWM2_CH1	P3.0	PIOCON2	PIO30	1	AUXR4[7:6]	PWM2C1P	00

PWM Channel	Output Pin	Control register 1			Control register2		
		SFR Byte Name	Bit name	Value	SFR Byte Name	Bit name	Value
	P3.1	PIOCON2	PIO31	1			01
	P0.0	PIOCON0	PIO00	1			10
	P0.4	PIOCON1	PIO04	1			11
PWM3_CH0	P3.2	PIOCON2	PIO32	1	AUXR5[1:0]	PWM3C0P	01
	P0.1	PIOCON0	PIO01	1			10
	P1.7	PIOCON1	PIO17	1			-
PWM3_CH1	P3.4	PIOCON2	PIO34	1	AUXR5[3:2]	PWM3C1P	01
	P1.5	PIOCON1	PIO15	1			10
	P0.3	PIOCON0	PIO03	1			11

Table 6.5-1 PWM Pin Define And Enable Control Register

6.6 Watchdog Timer (WDT)

6.6.1 Overview

The MS51 provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LIRC} \times \text{clock divider scalar}} \times 64$, where F_{LIRC} is the frequency of internal 10 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

WDPS.2	WDPS.1	WDPS.0	Clock Divider Scale	WDT Time-Out Timing[1]
0	0	0	1/1	6.40 ms
0	0	1	1/4	25.60 ms
0	1	0	1/8	51.20 ms
0	1	1	1/16	102.40 ms
1	0	0	1/32	204.80 ms
1	0	1	1/64	409.60 ms
1	1	0	1/128	819.20 ms
1	1	1	1/256	1.638 s
Note: This is an approximate value since the deviation of LIRC.				

Table 6.6-1 Watchdog Timer-out Interval Under Different Pre-scalars

Since the limitation of the maxima vaule of WDT timer delay. To up MS51 from idle mode or power down mode suggest use WKT function see Chapter 6.7 Self Wake-Up Timer (WKT).

6.7 Self Wake-Up Timer (WKT)

6.7.1 Overview

The MS51 has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has one clock source, internal 10 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 8-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

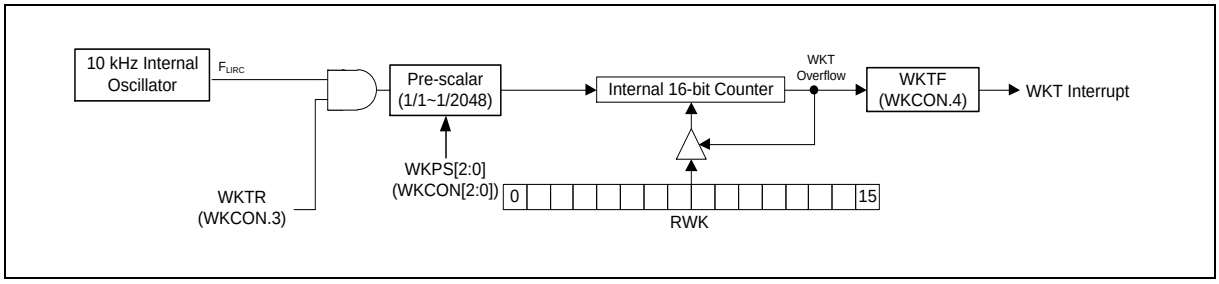


Figure 6.7-1 Self Wake-Up Timer Block Diagram

6.8 Serial Port (UART0 & UART1)

6.8.1 Overview

The MS51 includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

6.9 ISO 7816-3 Interface (SC0~2 & UART2 ~ 4)

6.9.1 Overview

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE provides ISO 7816-3 Interface controller (SC controller) with asynchronous protocal based on ISO/IEC 7816-3 standard. Software controls GPIO pins as the smartcard reset function and card detection function. This controller also provides UART emulation for high precision baud rate communication.

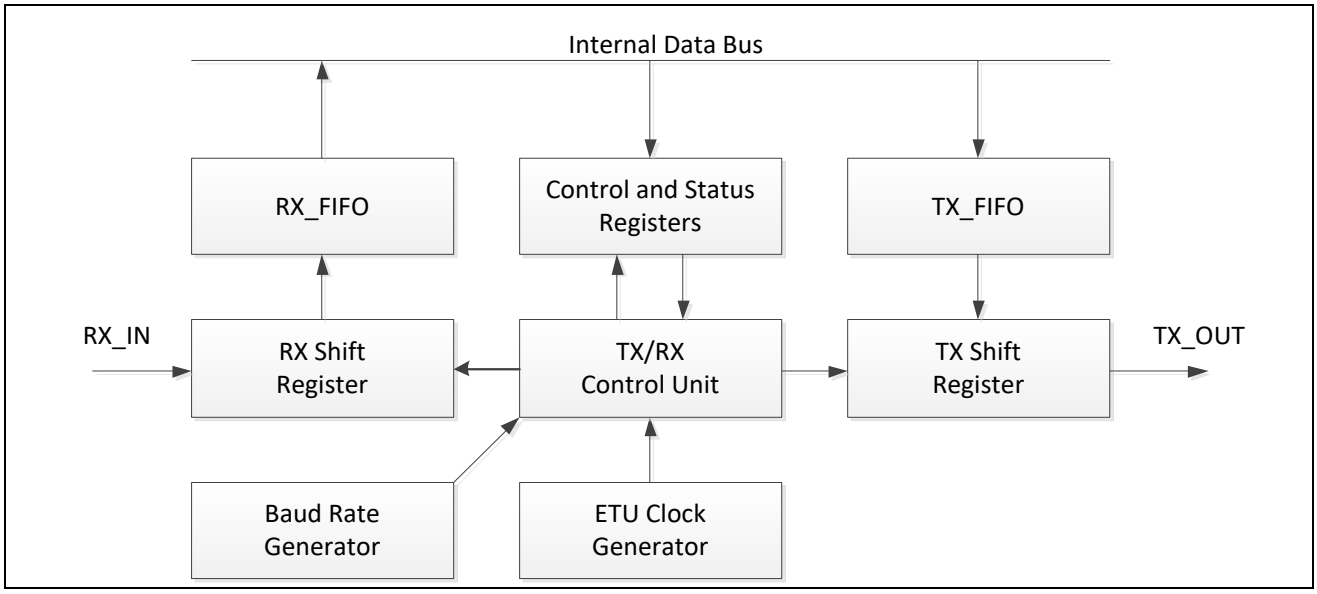


Figure 6.9-1 SC Controller Block Diagram

- ISO-7816-3 T = 0, T = 1 compliant
- Programmable transmission clock frequency
- Programmable extra guard time selection
- Supports auto inverse convention function
- Supports UART mode
  - Full duplex, asynchronous communications
  - Supports programmable baud rate generator for each channel
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCnEGT register
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

Following is the ISO 7816-3 multi function pin define

URAT Pin	SC Pin	Pin Name	SFR Define		
			SFR Byte Name	SFR Bit Name	Value
UART2_TXD	SC0_CLK	P0.3	AUXR2[7:6]	UART2TXP	01
		P3.0			10
UART2_RXD	SC0_DAT	P0.4	AUXR2[5:4]	UART2RXP	01
		P1.7			10

URAT Pin	SC Pin	Pin Name	SFR Define		
			SFR Byte Name	SFR Bit Name	Value
UART3_TXD	SC1_CLK	P1.2	AUXR3[3:2]	UART3TXP	01
		P1.5			10
		P0.5			11
UART3_RXD	SC1_DAT	P1.1	AUXR3[1:0]	UART3RXP	01
		P2.5			10
		P3.4			11
UART4_TXD	SC2_CLK	P2.3	AUXR3[7:6]	UART4TXP	01
UART4_RXD	SC2_DAT	P2.2	AUXR3[5:4]	UART4RXP	01

Table 6.9-1 Smart Card or UART Pin Define And Enable Control Register

6.10 Inter-Integrated Circuit (I^2C)

6.10.1 Overview

The MS51 provides two Inter-Integrated Circuit (I^2C) bus to serves as an serial interface between the microcontrollers and the I^2C devices such as EEPROM, LCD module, temperature sensor, and so on. The I^2C bus used two wires design (a serial data line I2C0_SDA and a serial clock line I2C0_SCL) to transfer information between devices.

The I^2C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I^2C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I^2C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I^2C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

6.11 Serial Peripheral Interface (SPI)

6.11.1 Overview

The MS51 provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to $F_{SYS}/2$, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

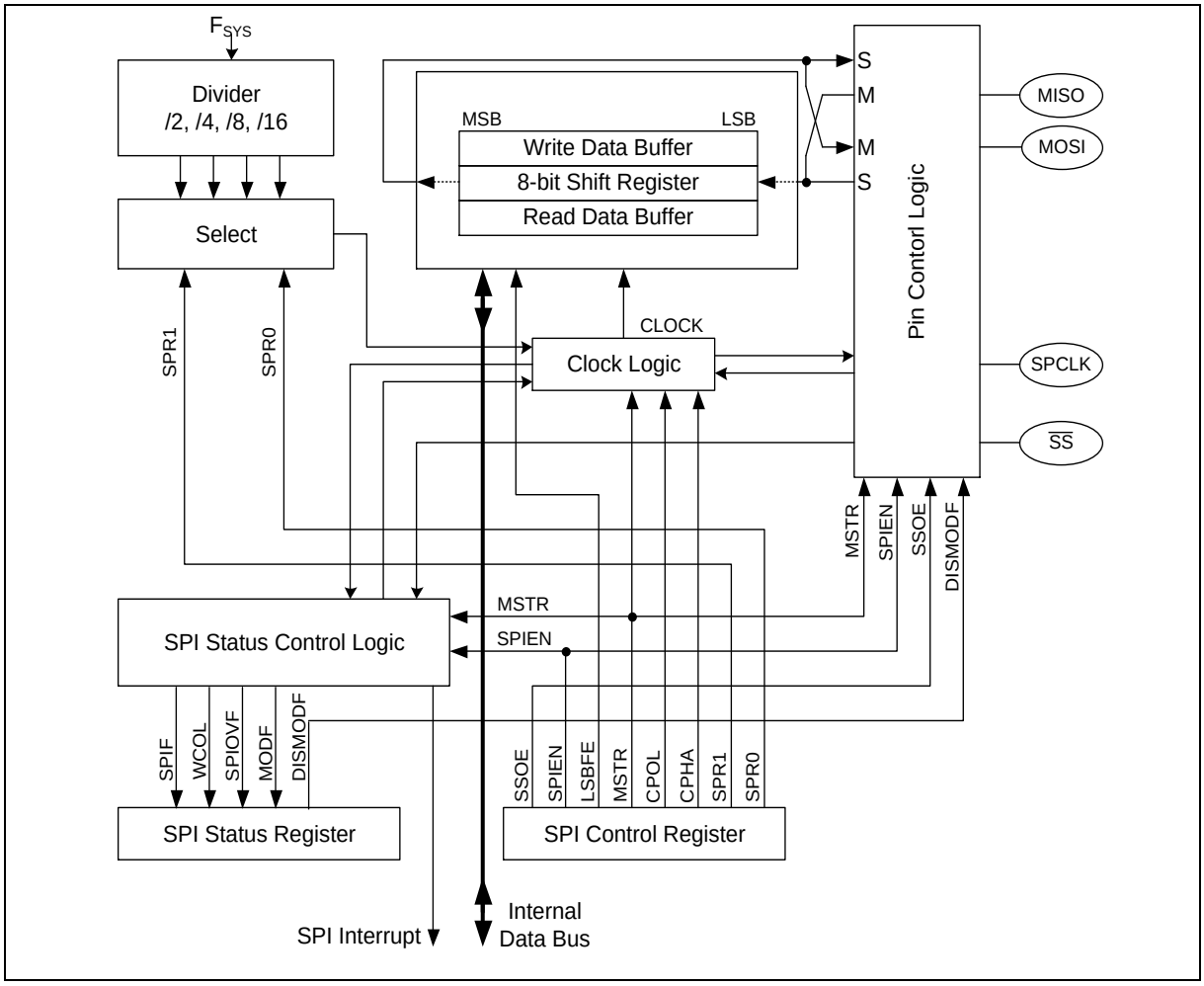


Figure 6.11-1 SPI Block Diagram

Figure15.1 SPI Block Diagram shows SPI block diagram. It provides an overview of SPI architecture in this device. The main blocks of SPI are the SPI control register logic, SPI status logic, clock rate control logic, and pin control logic. For a serial data transfer or receiving, The SPI block exists a write data buffer, a shift out register and a read data buffer. It is double buffered in the receiving and transmit directions. Transmit data can be written to the shifter until when the previous transfer is not complete. Receiving logic consists of parallel read data buffer so the shift register is free to accept a second data, as the first received data will be transferred to the read data buffer.

The four pins of SPI interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SPCLK), and Slave Select ($\overline{SS}$). The MOSI pin is used to transfer a 8-bit data in series from the Master to the Slave. Therefore, MOSI is an output pin for Master device and an input for Slave. Respectively, the MISO is used to receive a serial data from the Slave to the Master.

The SPCLK pin is the clock output in Master mode, but is the clock input in Slave mode. The shift clock is used to synchronize the data movement both in and out of the devices through their MOSI and MISO pins. The shift clock is driven by the Master mode device for eight clock cycles. Eight clocks exchange one byte data on the serial lines. For the shift clock is always produced out of the Master device, the system should never exist more than one device in Master mode for avoiding device conflict.

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). The signal should stay low for any Slave access. When $\overline{SS}$ is driven high, the Slave device will be inactivated. If the system is multi-slave, there should be only one Slave device selected at the same time. In the Master mode MCU, the $\overline{SS}$ pin does not function and it can be configured as a general purpose I/O. However, $\overline{SS}$ can be used as Master Mode Fault detection via software setting if multi-master environment exists. The MS51 also provides auto-activating function to toggle $\overline{SS}$ between each byte-transfer.

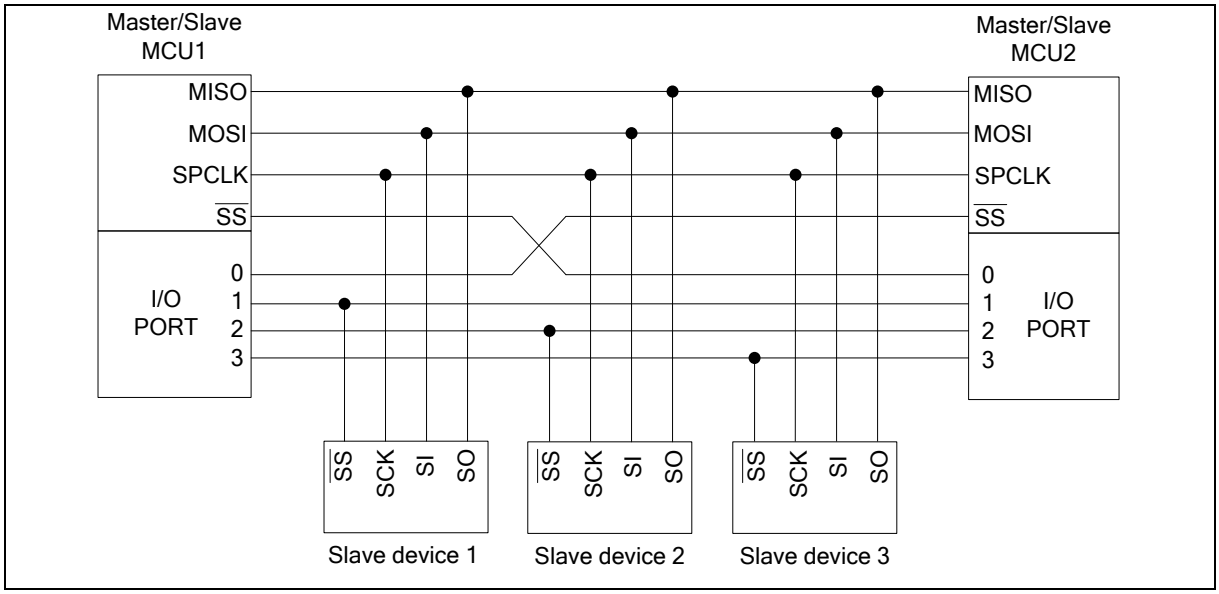


Figure 6.11-2 SPI Multi-Master, Multi-Slave Interconnection

Figure 6.11-2 shows a typical interconnection of SPI devices. The bus generally connects devices together through three signal wires, MOSI to MOSI, MISO to MISO, and SPCLK to SPCLK. The Master devices select the individual Slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins. MCU1 and MCU2 play either Master or Slave mode. The $\overline{SS}$ should be configured as Master Mode Fault detection to avoid multi-master conflict.

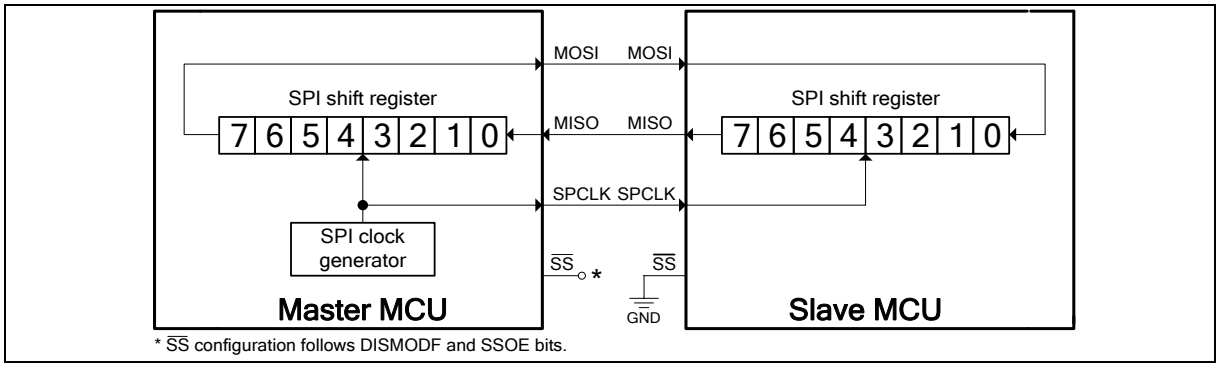


Figure 6.11-3 SPI Single-Master, Single-Slave Interconnection

Figure 6.11-3 shows the simplest SPI system interconnection, single-master and signal-slave. During a transfer, the Master shifts data out to the Slave via MOSI line. While simultaneously, the Master shifts

data in from the Slave via MISO line. The two shift registers in the Master MCU and the Slave MCU can be considered as one 16-bit circular shift register. Therefore, while a transfer data pushed from Master into Slave, the data in Slave will also be pulled in Master device respectively. The transfer effectively exchanges the data, which was in the SPI shift registers of the two MCUs.

By default, SPI data is transferred MSB first. If the LSBFE (SPCR.5) is set, SPI data shifts LSB first. This bit does not affect the position of the MSB and LSB in the data register. Note that all the following description and figures are under the condition of LSBFE logic 0. MSB is transmitted and received first.

There are three SPI registers to support its operations, including SPI control register (SPCR), SPI status register (SPSR), and SPI data register (SPDR). These registers provide control, status, data storage functions, and clock rate selection. The following registers relate to SPI function.

6.12 12-Bit Analog-To-Digital Converter (ADC)

6.12.1 Overview

The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE is embedded with a 12-bit SAR ADC. The ADC (analog-to-digital converter) allows conversion of an analog input signal to a 12-bit binary representation of that signal. The MS51EB0AE / MS51FC0AE / MS51XC0BE / MS51EC0AE / MS51TC0AE / MS51PC0AE is selected as 8-channel inputs in single end mode. The internal band-gap voltage 1.22 V also can be the internal ADC input. The analog input, multiplexed into one sample and hold circuit, charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation and stores the result in the result registers. The ADC controller also supports continuous conversion and storage result data into XRAM.

7 APPLICATION CIRCUIT

7.1 Power supply scheme

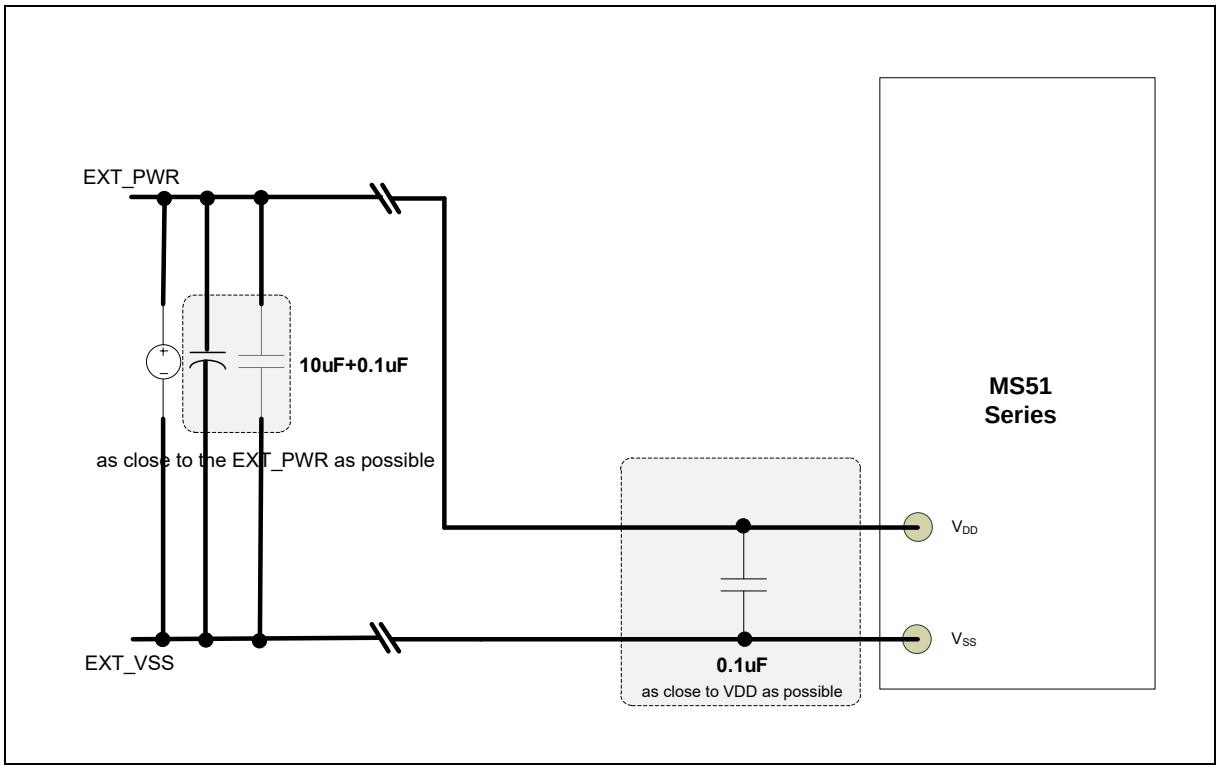
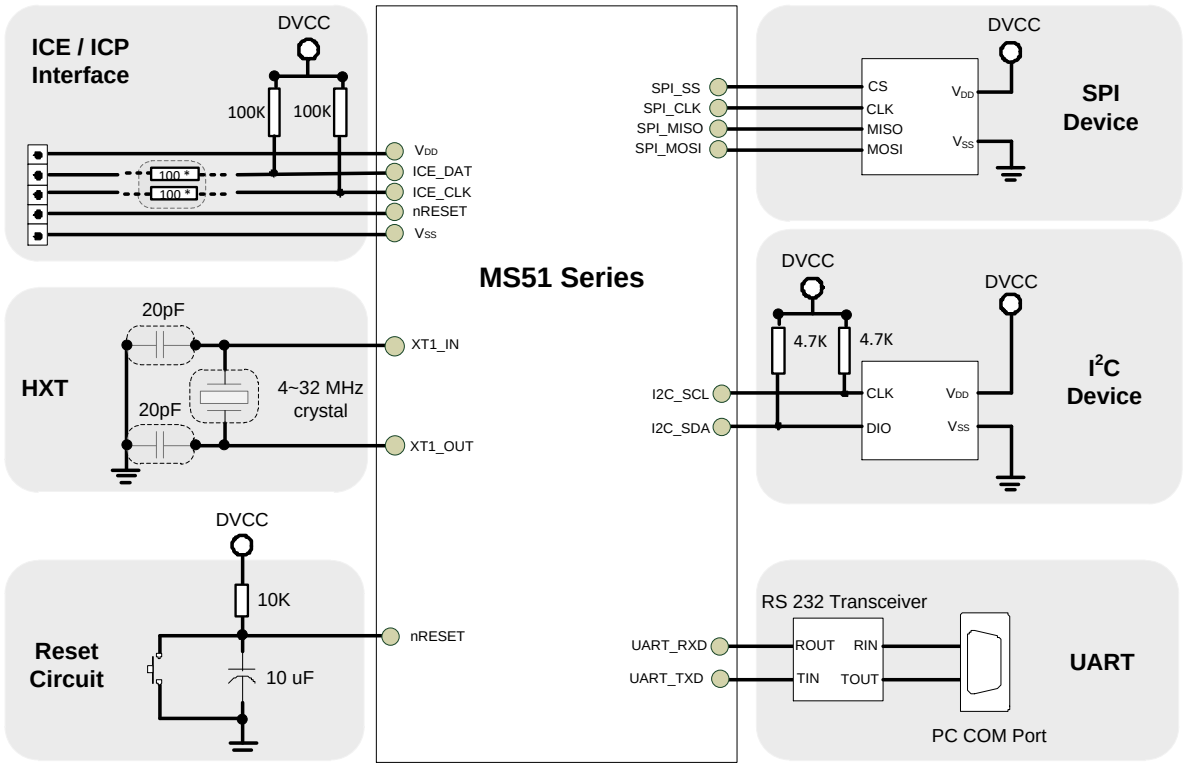


Figure 7.1-1 NuMicro® MS51 Power supply circuit

7.2 Peripheral Application scheme



*ICE/ICP interface ICE_DAT/ICE_CLK pin 100ohm resister is selectable only for filter the disturb of noise on the circuit.

Note:

1. It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.
2. It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
3. It is optional add 100ohm resistor series between ICE_DAT/ICE_CLK pin to help filtering noise interference.
4. The HXT external capacitor value please reference Section 8.3.2.2 Typical Crystal Application Circuits Capacitors Value

Figure 7.2-1 NuMicro® MS51 Peripheral interface circuit

8 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the MS51 electrical characteristics.

8.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 8.1-1 General operating conditions

8.2 DC Electrical Characteristics

8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	3.6	4.2	4.6	4.8	mA
		24 MHz(HIRC)[1] @3.3V	3.2				
		24 MHz(HIRC)[1] @2.4V	2.9				
		16 MHz (HIRC) [1] @5.5V	3.3	3.4	3.9	4.6	
		16 MHz (HIRC) [1] @3.3V	3.1				
		16 MHz (HIRC) [1] @2.4V	2.8				
		10 kHz (LIRC)[2]	0.30	0.32	0.46	2.33	

Notes:

1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 Current consumption in Normal Run mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.8	2.9	3.2	3.8	mA
		24 MHz(HIRC)[1] @3.3V	2.4				
		24 MHz(HIRC)[1] @2.4V	2.2				
		16 MHz (HIRC)[1] @5.5V	2.2	2.5	2.6	3.2	
		16 MHz (HIRC)[1] @3.3V	1.9				
		16 MHz (HIRC)[1] @2.4V	1.8				
		10 kHz (LIRC)[2]	0.3	0.5	0.9	2.3	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-2 Current consumption in Idle mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@5.5V	6.5	6.2	9	55	µA
	Power down mode, all peripherals disable@3.3V	6				
	Power down mode, all peripherals disable@2.4V	5.8				
	Power down mode, LVR enable all other peripherals disable	7.5	6.7	10[3]	57	
	Power down mode, LVR enable BOD enable all other peripherals disable	180	165	197	292	

Notes:
1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 8.2-3 Chip Current Consumption in Power down mode

8.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	30	µs
		Fsys = HIRC @ 24MHz		30	µs

Notes:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 8.2-4 Low-power mode wakeup timings

8.2.3 I/O DC Characteristics

8.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IL1}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	$0.2V_{DD}$-0.1	V	
V_{IH}	Input high voltage	$0.2V_{DD}$+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.2-5 I/O input characteristics

8.2.3.2 I/O Output Characteristics

The minimum and maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and temperature condition is T_A= 25 °C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	μA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	μA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	12.5	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
V_{OH}[1]	Output high level voltage for quasi-bidirectional mode	V_{DD}-0.4	-	V_{DD}	V	I_{SR} = -7.3 uA
	Output high level voltage for push-pull mode	V_{DD}-1.2	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -20 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -13 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -9 mA
		V_{DD}-0.4	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -9 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -6 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -4.2 mA

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}[1]	Output low level voltage for push-pull mode	V_{SS}	-	1.2	V	V_{DD} ≥ 2.7 V I_{SR} = 20 mA (Max.)
		V_{SS}	-	0.4	V	V_{DD} ≥ 5.5 V I_{SR} = 18 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = 16 mA
					V	V_{DD} ≥ 2.4 V I_{SR} = 9.7 mA
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.2-6 I/O output characteristics

8.2.3.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.2-7 nRESET Input Characteristics

8.3 AC Electrical Characteristics

8.3.1 Internal High Speed RC Oscillator (HIRC)

8.3.1.1 16MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20 °C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40 °C ~ -20 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.3.1.2 24MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-2 24MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.3.2 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions[2]
V_{DD}	Operating voltage	1.8	-	5.5	V	
R_f	Internal feedback resister	-	500	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	80	180	µA	4 MHz, Gain = L0
		-	110	300		8 MHz, Gain = L1
		-	180	500		12 MHz, Gain = L2
		-	230	650		16 Mhz, Gain = L3
		-	360	975		24 MHz, Gain = L4
T_S	Stable time	-	3500	3700	µs	4 MHz, Gain = L0
		-	950	1050		8 MHz, Gain = L1
		-	700	850		12 MHz, Gain = L2
		-	450	550		16 Mhz, Gain = L3
		-	400	570		24 MHz, Gain = L4
Du_{HXT}	Duty cycle	40	-	60	%	

Notes:
1. Guaranteed by characterization, not tested in production.
2. L0 ~ L4 defined by SFR XLTCON[6:4] HXSG

Table 8.3-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

8.3.2.2 Typical Crystal Application Circuits Capacitors Value

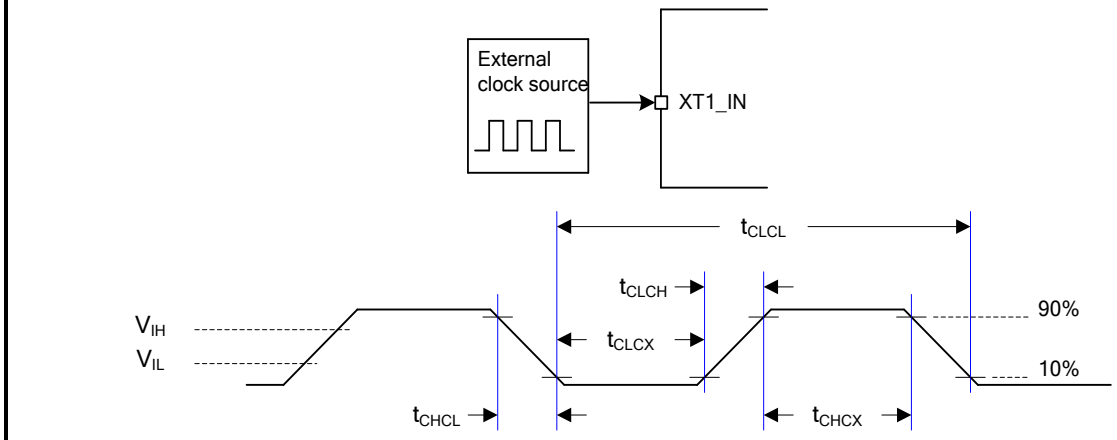
For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 25 pF	10 ~ 25 pF	without

8.3.3 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.3-4 External 4~24 MHz High Speed Clock Input Signal

8.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 8.3-5 10 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

8.3.5 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 8.3-6 I/O AC characteristics

8.4 Analog Characteristics

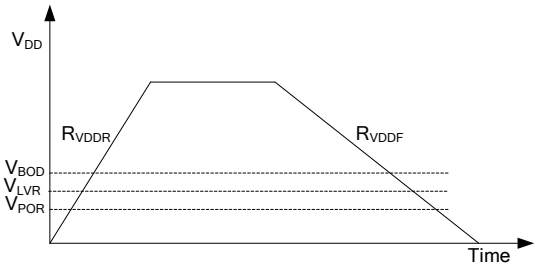
8.4.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1	1.15	1.3	V	-
V_{LVR}	LVR reset voltage	1.7	2.0	2.4		-
V_{BOD}	BOD brown-out detect voltage	4.10	4.4	4.70		BOV[1:0] = [0,0]
		3.50	3.7	3.90		BOV[1:0] = [0,1]
		2.50	2.7	2.90		BOV[1:0] = [1,0]
		2.00	2.2	2.40		BOV[1:0] = [1,1]
T_{LVR_SU}[*1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC@16MHz
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz

Notes:
1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.4-1 Reset and power control unit



BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 8.4-2 Minimum Brown-out Detect Pulse Width

8.4.2 12-bit SAR ADC

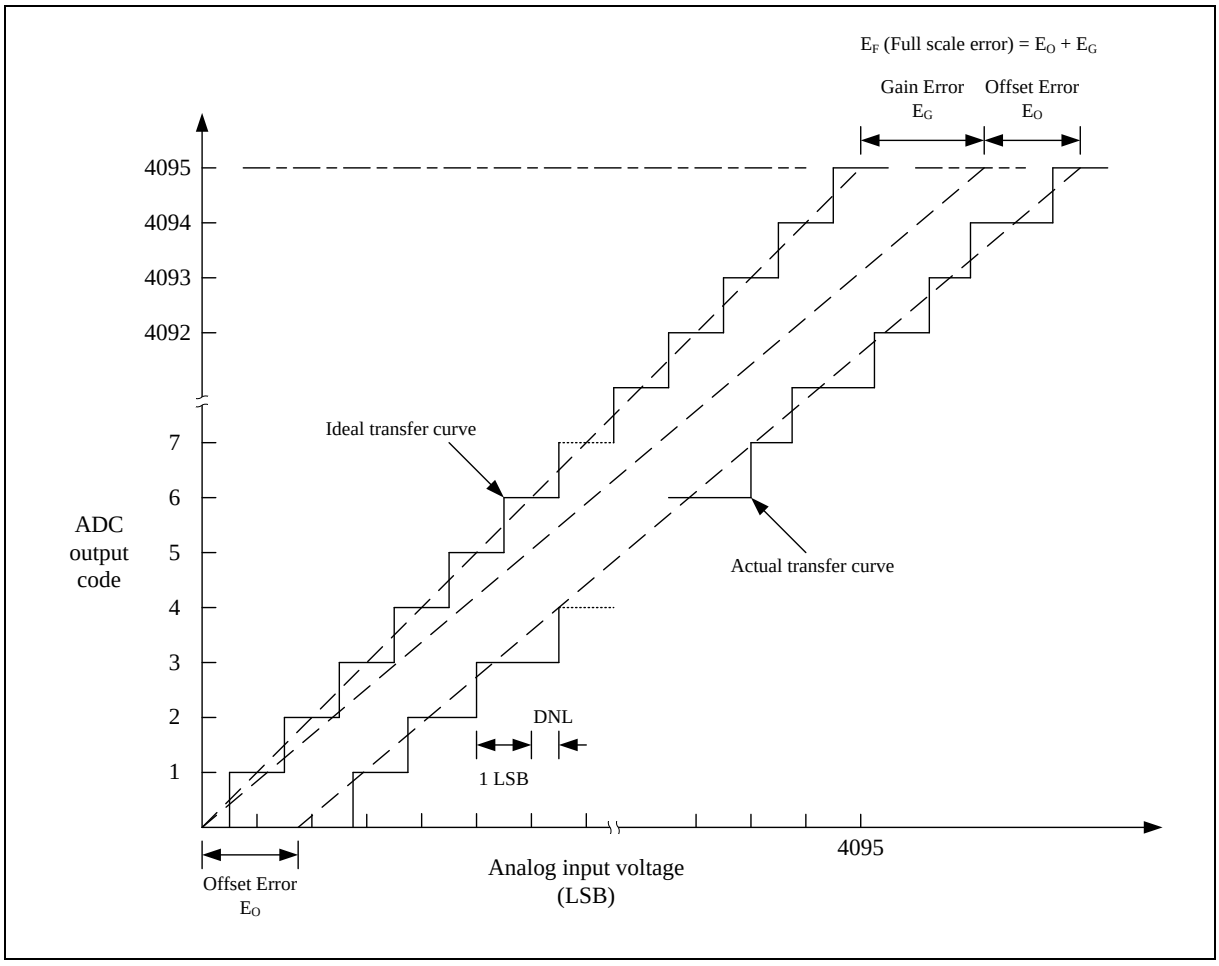
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 500 kHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADCEC}[1]	Encoding Rate	500			kHz	This value is fixed by ADC module
T_{ADCEC}	Encoding Time	2			μs	This value is fixed by ADC module
F_{ADCSMP}[1]	ADC Sampling Clock frequency	F_{SYS}/8		F_{SYS}	kHz	base on ADCDIV (ADCCON1[5:4]
T_{ADCSMP}	ADC Sampling Time [2]z	0.375	-	17	μs	F_{SYS} = 16MHz;
		0.417	-	11.3	μs	Fsys = 24MHz; ADCAQT = 1 by software[3]
F_{ADCCOV}	Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$	52.6	-	421	kHz	F_{SYS} = 16MHz;
		75.2	-	413	kHz	F_{SYS} = 24MHz;
T_{ADCCOV}[2]	Conversion Time $T_{ADCCOV} = T_{SMP} + T_{ADCEC}$	2.375	-	19	μs	F_{SYS} = 16MHz;
		2.417	-	13.3	μs	F_{SYS} = 24MHz;
T_{ADCEN}	ADC Enable to ready time	20	-	-	μs	
INL[1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[1]	Gain error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_O[1]$_T$	Offset error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[1]	Absolute Error	-7	-	+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$
R_S	Input Channel Equivalent Resistance	-	0.5	2.5	kΩ	
C_{IN}	Input Equivalent Capacitance	-	2.5	-	pF	

1. Guaranteed by characterization result, not tested in production.
2. ADC Convertion time T_{ADCCOV} = ADC Sampling Time (T_{SMP}) + ADC Encoding Time (T_{ADCEC}).
3. ADC Sampling Time $T_{SMP} = \frac{4 * ADCAQT + 6}{F_{ADCSMP}}$ （F_{ADCSMP} base on ADCDIV (ADCCON1[5:4])

   If F_{SYS} = 16MHz, ADC Sampling Time Minimum condition $\frac{6}{16MHz}$ (ADCAQT = 0, ADCDIV = 0), ADC Sampling Time Maximum condition $\frac{4*7+6}{16MHz/8}$ (ADCAQT = 7, ADCDIV = 8)

   If F_{SYS} = 24MHz, ADC Sampling Time Minimum condition $\frac{4*1+6}{24MHz}$ (ADCAQT = 1, ADCDIV = 0), Since the minimum sampling time must over 370ns that means when F_{ADCAQT} = 24MHz, ADCAQT must be set as 1 by software at least.

Table 8.4-3 ADC characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5 Communications Characteristics

8.5.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	$F_{SYS}/2$	MHz	2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	$1/F_{SYS}$	-	-	ns	
t_V	Data output valid time	-	-	5	ns	Matser mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
				$1/F_{SYS}$	ns	Slave mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.5-1 SPI Master Mode Characteristics

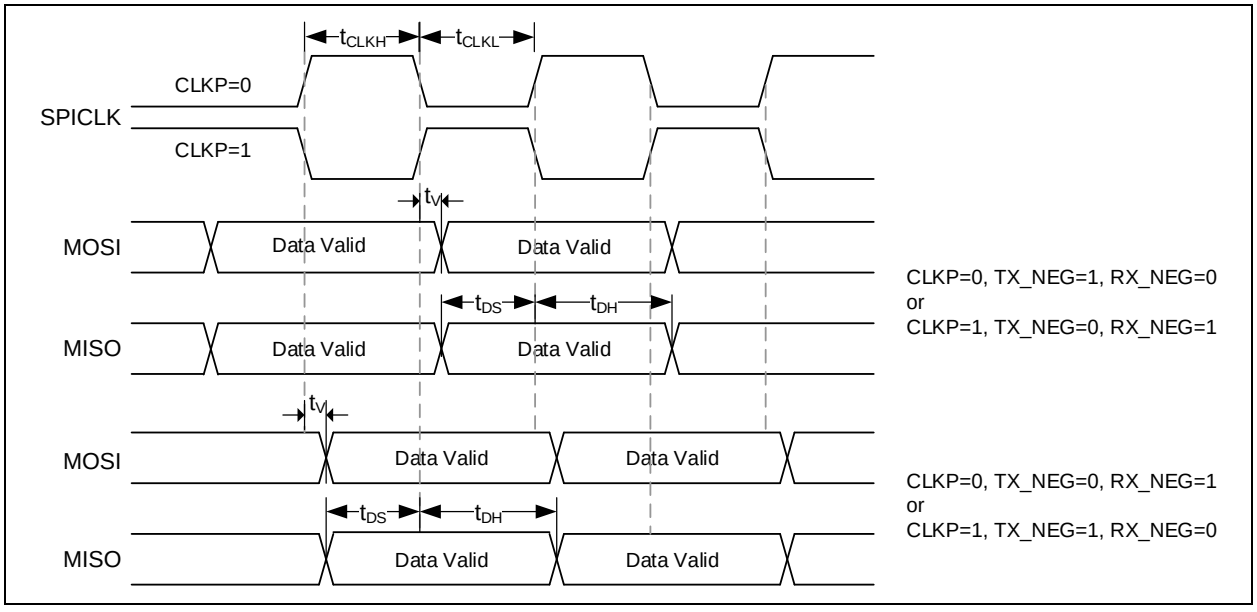


Figure 8.5-1 SPI Master Mode Timing Diagram

8.5.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	$8F_{SYS}$[5]	0[4]	$8F_{SYS}$[5]	µs
t_r	SCL/SDA rise time	-	1000	$20+0.1C_b$	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 4 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 16 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.5-2 I²C Characteristics

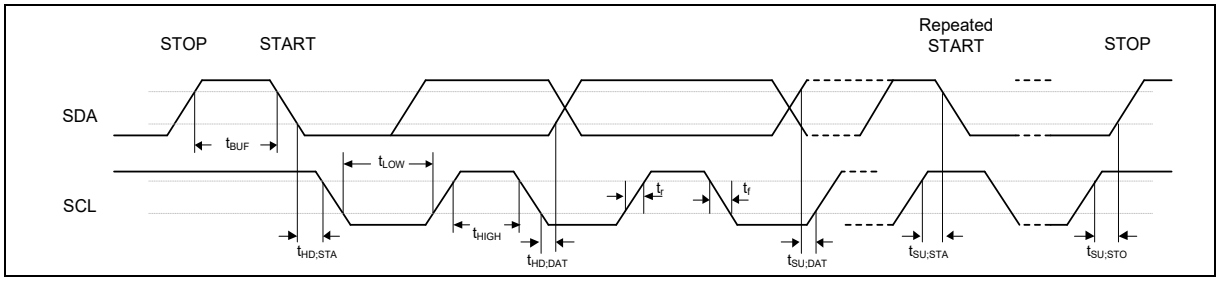


Figure 8.5-2 I²C Timing Diagram

8.6 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25℃
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55℃
		25	-	-	year	100 kcycle[3] T_A = 85℃
		10	-	-	year	100 kcycle[3] T_A = 105℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.6-1 Flash memory characteristics

8.7 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.7.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:
1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 8.7-1 Voltage characteristics

8.7.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:
1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.7-2 Current characteristics

8.7.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	°C/Watt
	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	°C/Watt
	Thermal resistance junction-ambient 28-pin TSSOP(4.4x9.7 mm)		30	-	°C/Watt
	Thermal resistance junction-ambient 32-pin LQFP(7x7 mm)		62	-	°C/Watt
	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)		28	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.7-3 Thermal characteristics

8.7.4 EMC Characteristics

8.7.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.7.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.7.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.7-4 EMC characteristics

8.7.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge[1]	MSL
20-pin QFN(3x3 mm)	MSL 3
20-pin TSSOP(4.4x6.5 mm)	MSL 3
28-pin TSSOP (4.4 x 9.7 x 1.0 mm)	MSL 3
32-pin LQFP (7.0 x 7.0 x 1.4 mm)	MSL 3
33-pin QFN (4.0 x 4.0 x0.8 mm)	MSL 3

Note:
1. Determined according to IPC/JEDEC J-STD-020

Table 8.7-5 Package Moisture Sensitivity(MSL)

8.7.6 Soldering Profile

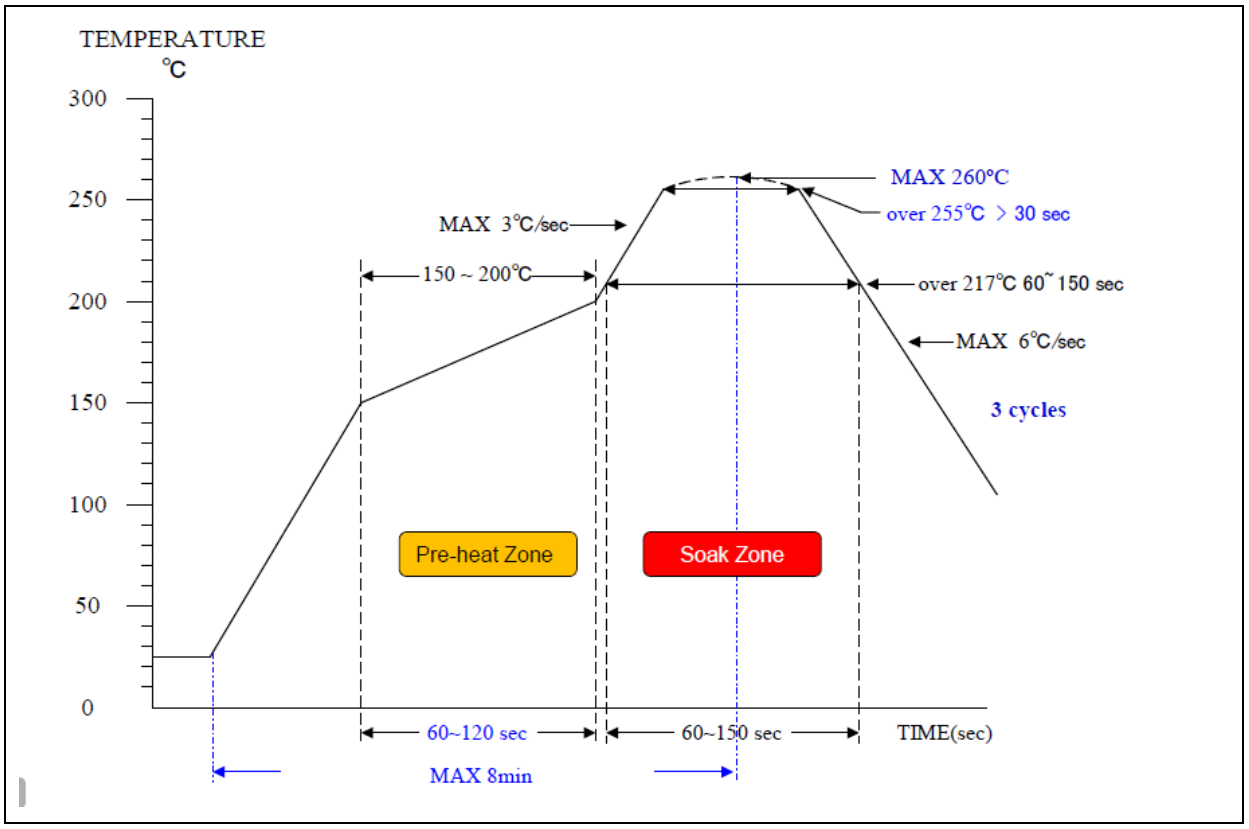


Figure 8.7-1 Soldering profile from J-STD-020C

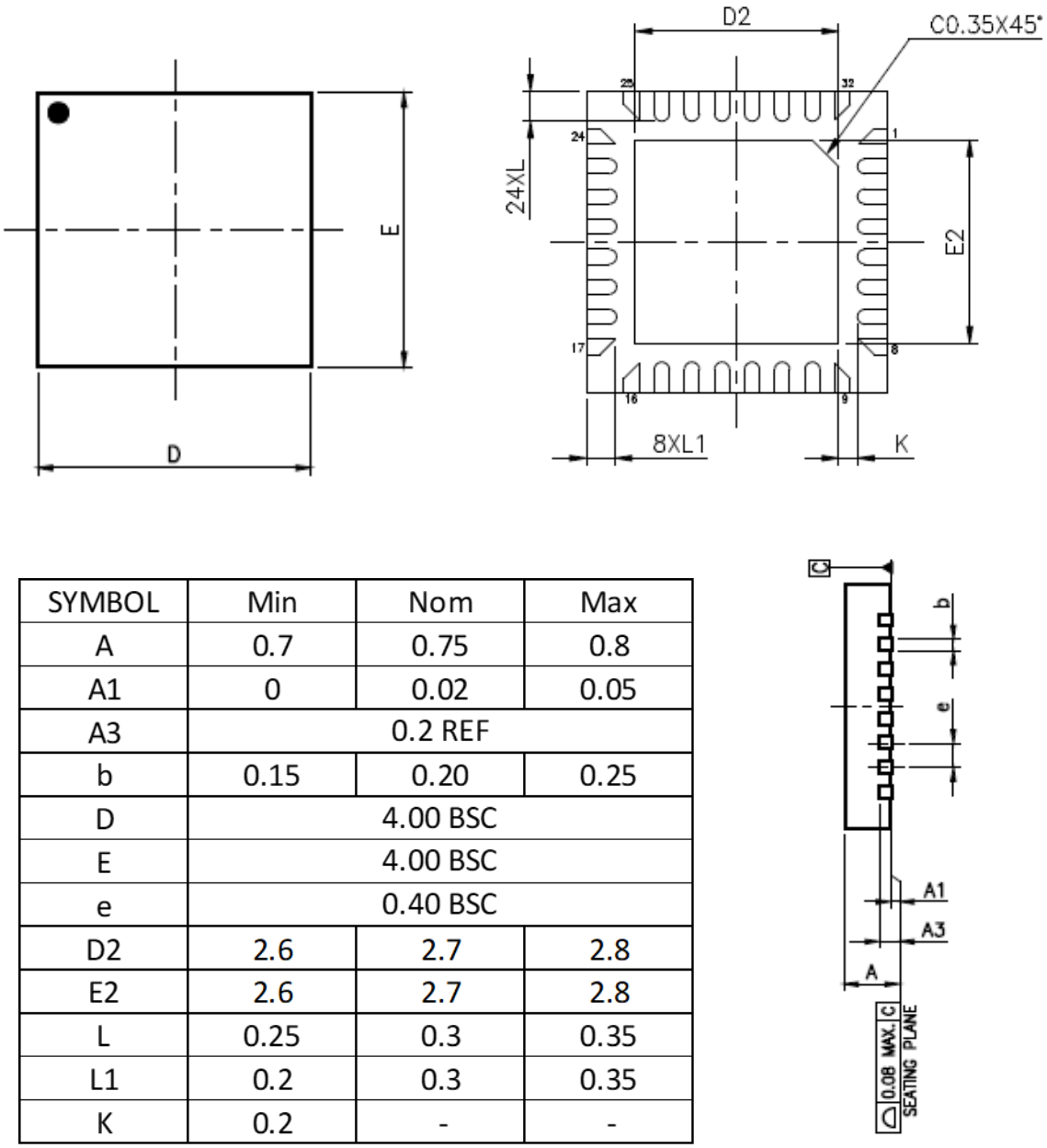
Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.7-6 Soldering Profile

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

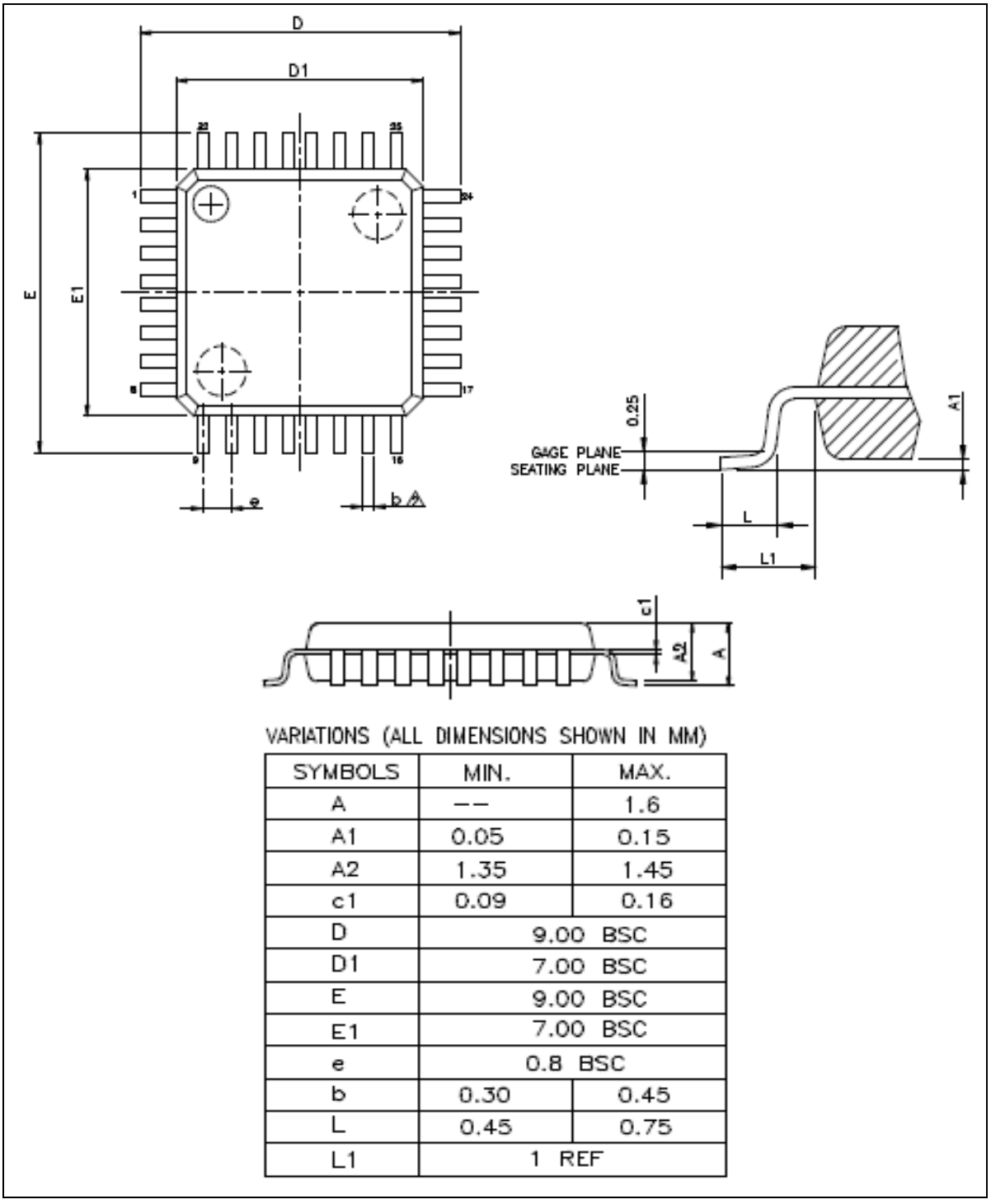
9.1 QFN 33-pin (4.0 x 4.0 x 0.8 mm)



SYMBOL	Min	Nom	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3		0.2 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.6	2.7	2.8
E2	2.6	2.7	2.8
L	0.25	0.3	0.35
L1	0.2	0.3	0.35
K	0.2	-	-

Figure 9.1-1 QFN-33 Package Dimension

9.2 LQFP 32-pin (7.0 x 7.0 x 1.4 mm)

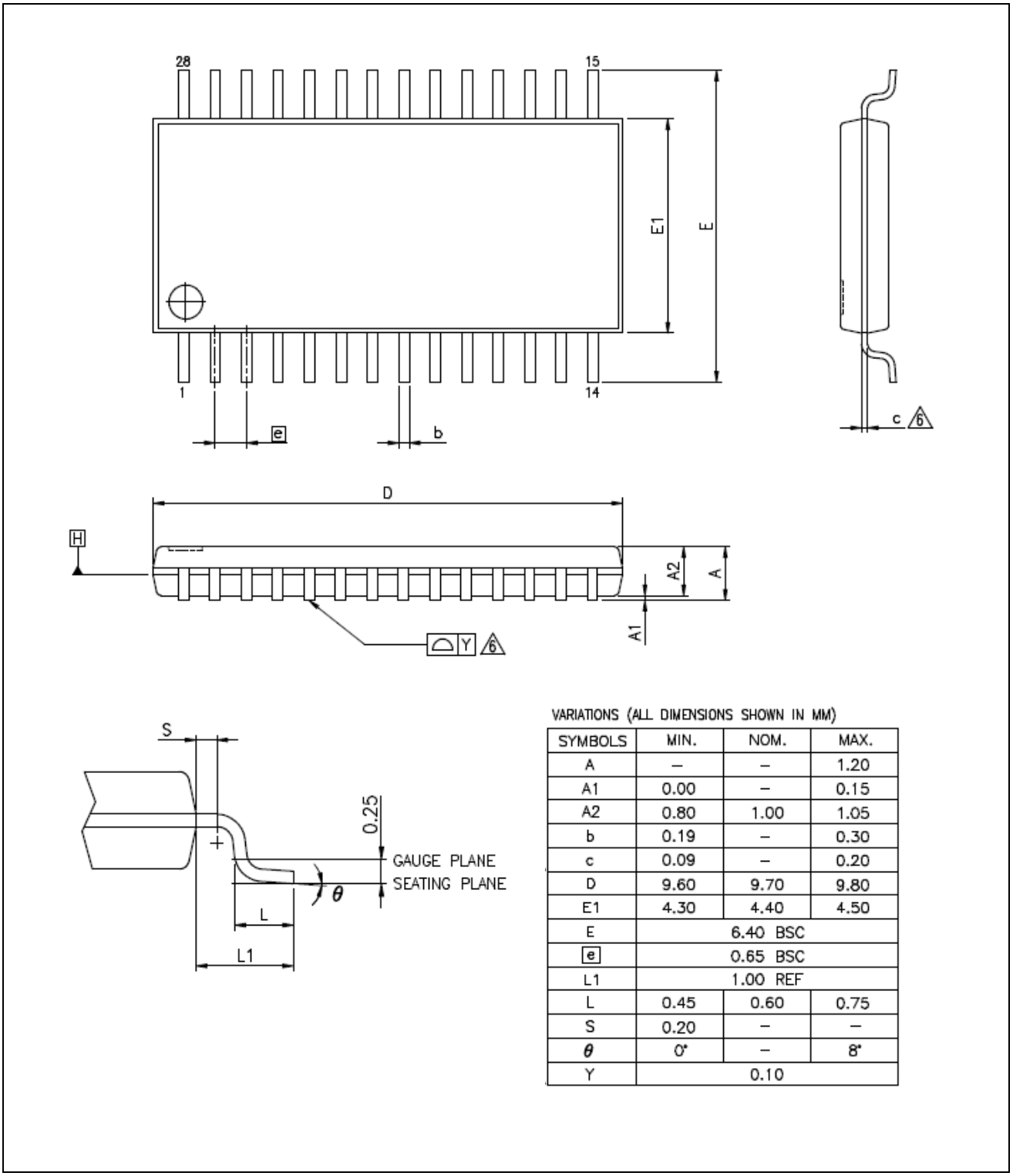


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.8 BSC	
b	0.30	0.45
L	0.45	0.75
L1	1 REF	

Figure 9.2-1 LQFP-32 Package Dimension

9.3 TSSOP 28-pin (4.4 x 9.7 x 1.0 mm)

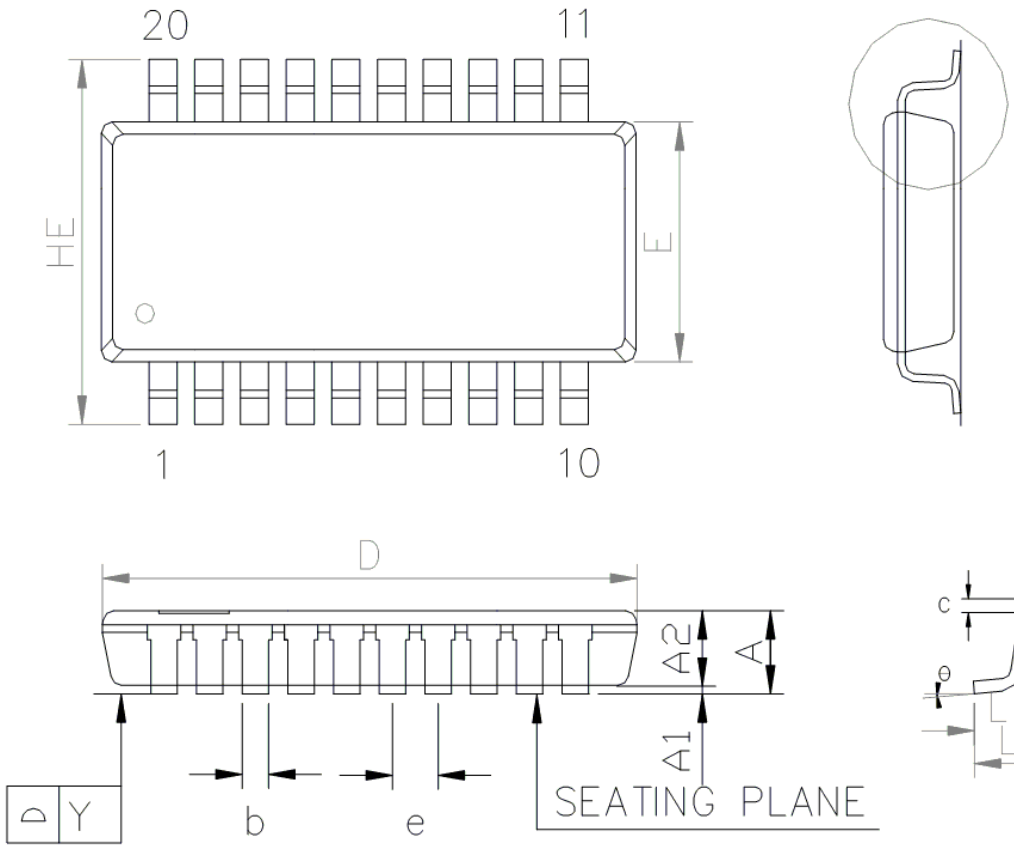


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

Figure 9.3-1 TSSOP-28 Package Dimension

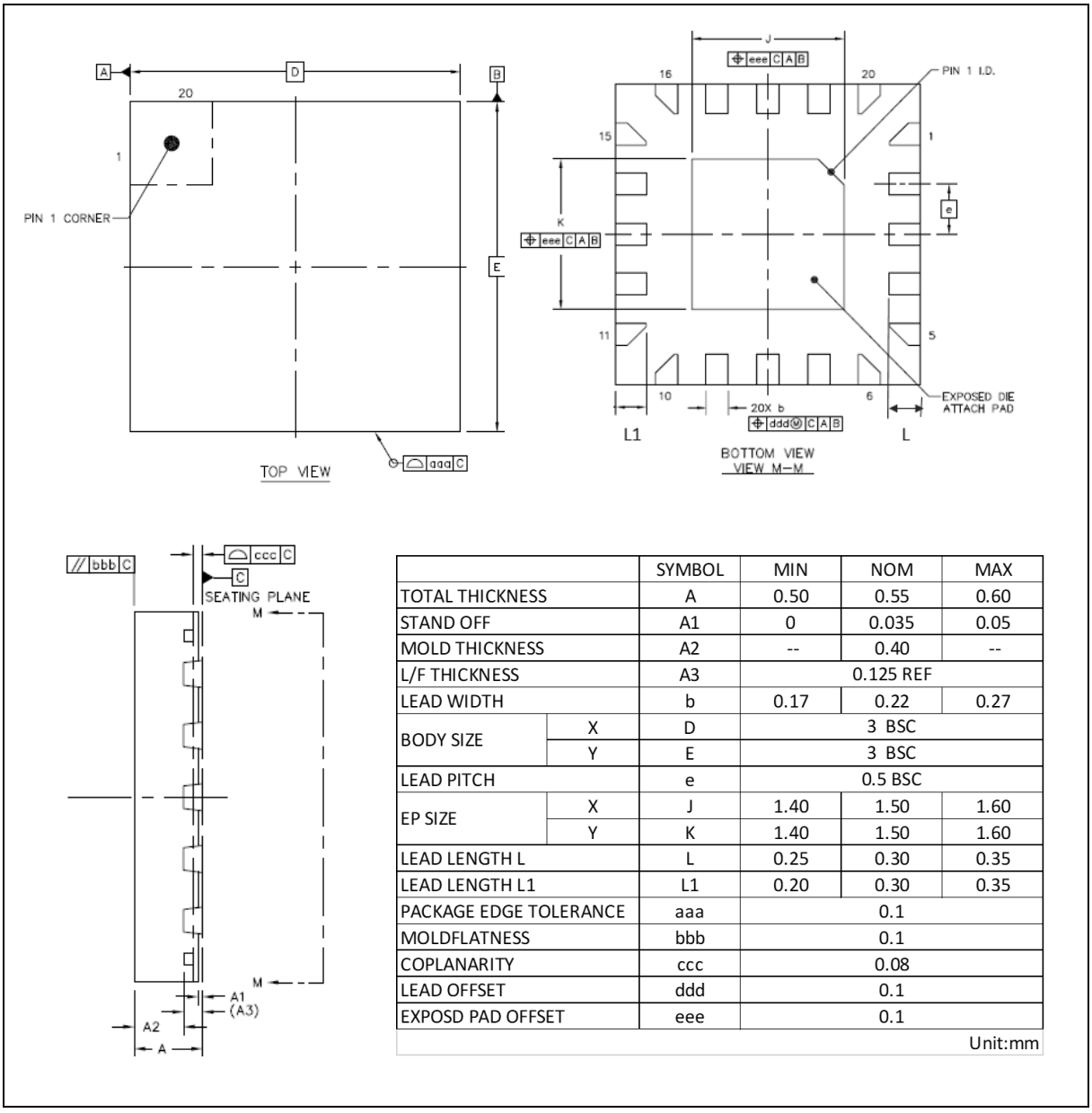
9.4 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE		6.40 BSC			0.252 BSC	
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF			0.039 REF	
b	0.19	-	0.30	0.007	-	0.012
e		0.65 BSC			0.026 BSC	
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y		0.10 BASIC			0.004 BASIC	

Figure 9.4-1 TSSOP-20 Package Dimension

9.5 QFN 20-pin (3.0 x 3.0 x 0.6mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.50	0.55	0.60
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	--	0.40	--
L/F THICKNESS		A3		0.125 REF	
LEAD WIDTH		b	0.17	0.22	0.27
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	1.40	1.50	1.60
	Y	K	1.40	1.50	1.60
LEAD LENGTH L		L	0.25	0.30	0.35
LEAD LENGTH L1		L1	0.20	0.30	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLDFLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSD PAD OFFSET		eee		0.1	

Unit:mm

Figure 9.5-1 QFN-20 Package Dimension for MS51XC0BE

10 ABBREVIATIONS

10.1 Abbreviations List

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description	
2019.11.28	1.00		Initial release
2019.12.25	1.01	Section 3.2	Modified selection guide table MS51FC0AE/MS51XC0BE ISO 7816-3 number to 2. Added description for MS51FC0AE.
		Section 4.2	Added P3.0 PWM2_CH1 pin define in Pin Description table.
		Section 8.6.4	Modified EFT level to 4.4kV
2021.02.25	1.02	Section 3.2	Added description for MS51EB0AE.
		Section 8.4.2	Added ADC sampling timing data of F_{SYS} = 24MHz.
		Section 9.1	Modified QFN33 package dimension to add lead length L1 condition.
		Section 9.5	Modified QFN20 package dimension to add lead length L1 condition.
2022.02.08	1.03	Section 4.2	Added QFN-20 pin EPAD descritpion.
		Section 8.4.2	Added ADC input equivalent resistance and capacitance value. Modified ADC convert time description..
2023.02.15	1.04	Section 4.2	Added notes about the hardware reference design for ICE_DAT, ICE_CLK and nRESET pins
		Section 8.2.3.2	Modified I_{SK} Maximum value from 11mA to 12.5 mA.
			Added R_{PU} and R_{PD} Resistor value
		Section 8.5	Added Communication Characteristics include SPI and I^2C.
		Section 8.6.2	Added I_{INJ}(PIN) and ΣI_{INJ}(PIN) Current value
2023.06.05	1.05	Section 4.1	Modified P3.6 and P3.7 description in Pin Description table.
			Added P1.7 PWM3_CH0 description.
		Section 8.2.2	Added power down entry time description in note.
		Section 8.4.1	Modified BOD brown-out detect voltage Range.

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